
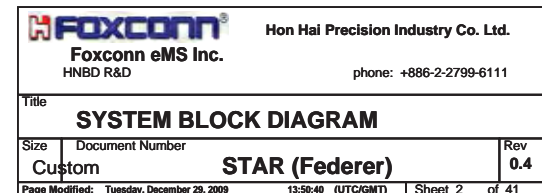
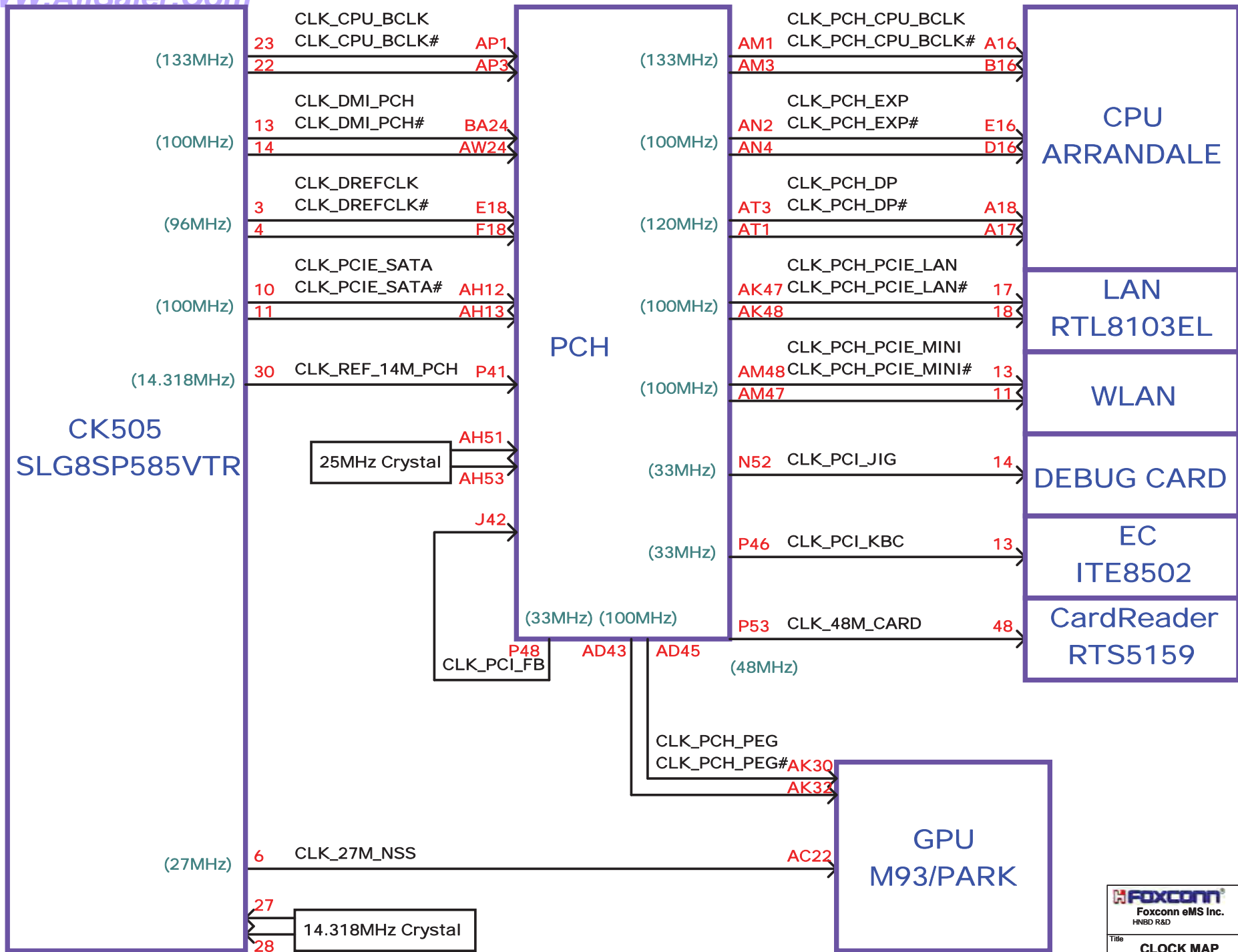


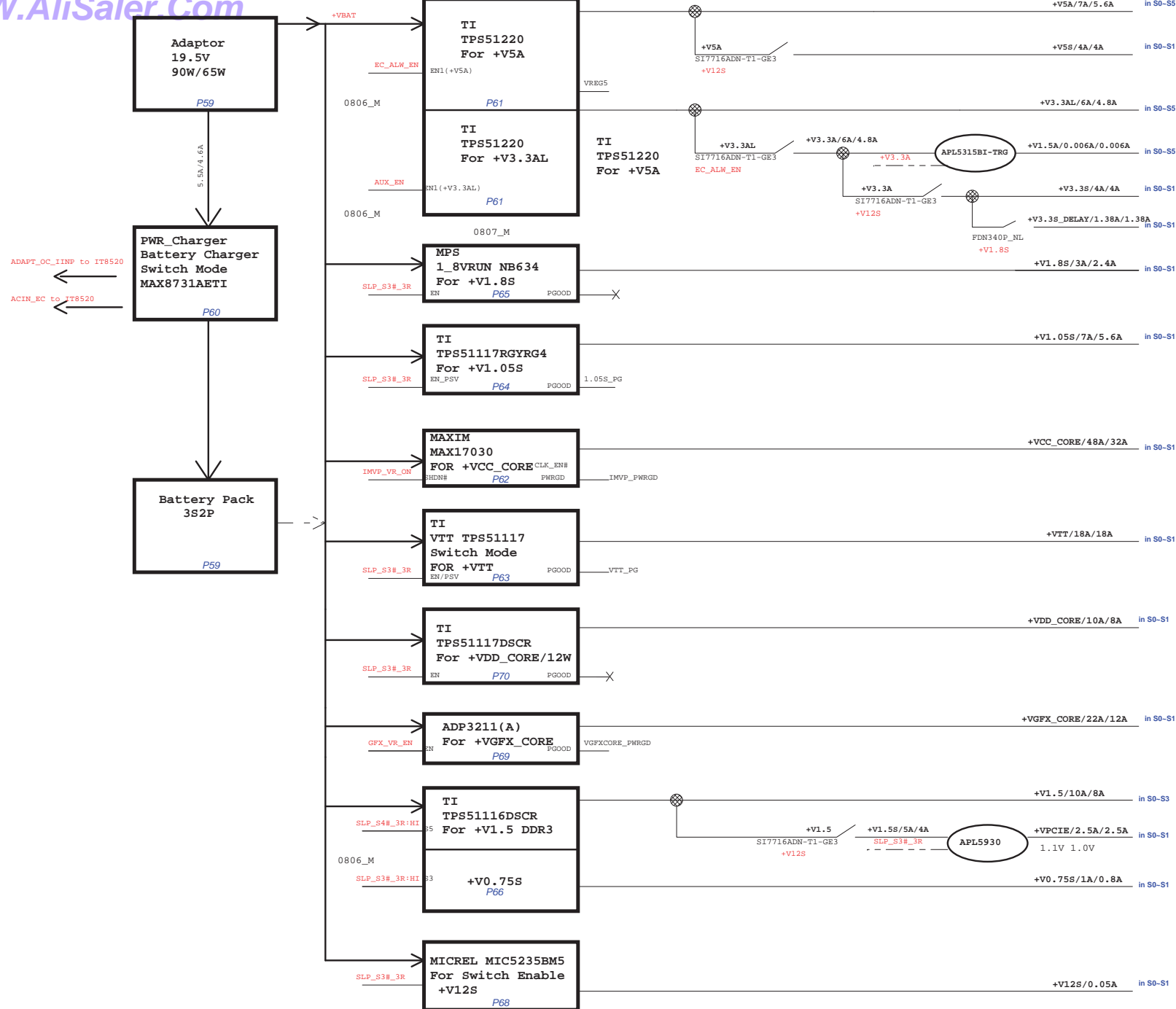
01 -- COVER SHEET	21 -- VGA_S3 (IO) 2/5
02 -- SYSTEM BLOCK DIAGRAM	22 -- VGA_S3 (DDR3) 3/5
03 -- CLOCK MAP	23 -- VGA_S3 (DP) 4/5
04 -- POWER MAP	24 -- VGA_S3 (POWER) 5/5
05 -- POWER SEQUENCY DIAGRAM	25 -- VRAM (DDR3)
06 -- POWER SEQUENCY TIMING	26 -- EC+KBC (IT8502E)
07 -- SMBUS MAP	27 -- CODEC/JACK/SPEAKER/MIC
08 -- RESET SIGNAL MAP	28 -- LAN (RTL8103EL)/CLOCK GEN
09 -- Calpella (DMI,PEG,FDI)	29 -- Card Reader
10 -- Calpella (CLK,MISC,JTAG)	30 -- WLAN/BT/MDC/USB/MOUNTING
11 -- Calpella (DDR3)	31 -- LVDS/CRT/Webcam
12 -- Calpella (POWER/GND)	32 -- HDMI
13 -- Calpella (GRAPHIC POWER)	33 -- DCIN/Battery/OCP/FAN
14 -- PCH (HDA,JTAG,SATA)	34 -- PWR_Charger MAX8731AETI
15 -- PCH (PCI-E,SMBUS,CLK)	35 -- 5V/3.3V SN0608098RHB
16 -- PCH (DMI,FDI,GPIO,LVDS)	36 -- Vcore MAX17030
17 -- PCH (PCI,USB,NVRAM,GPIO)	37 -- 1.1V VTT/+V1.05RUN
18 -- PCH (POWER)	38 -- 1.5VDDR3+0.75V+V1.8RUN
19 -- DDR3(SO-DIMM_0&1)	39 -- PWR_Others power plane
20 -- VGA (PCI-E/STRAP) 1/5	40 -- CPU VREG & Decoupling
	41 -- ATVDD/+VPCIE

P. Leader	Check by	Design by

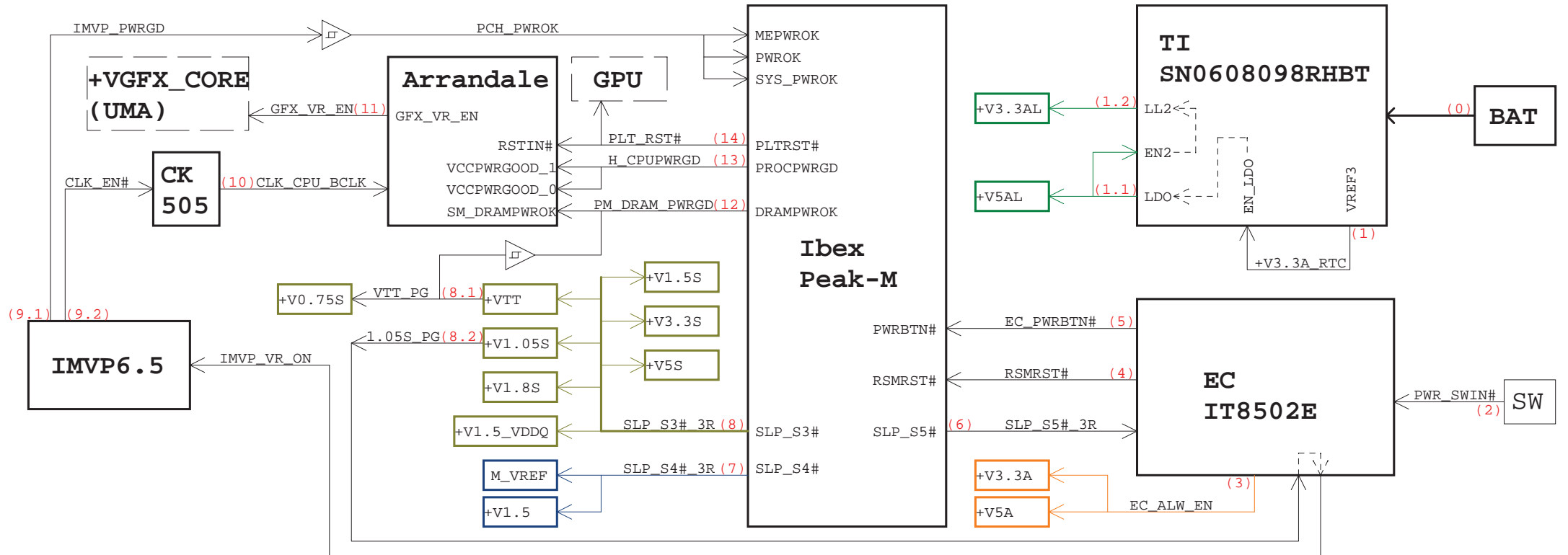
 Foxconn EMS Inc. HNBD R&D		Hon Hai Precision Industry Co. Ltd. phone: +886-2-2799-6111
Title		
Index Page		
Size	Document Number	Rev
Custom	STAR (Federer)	0.4
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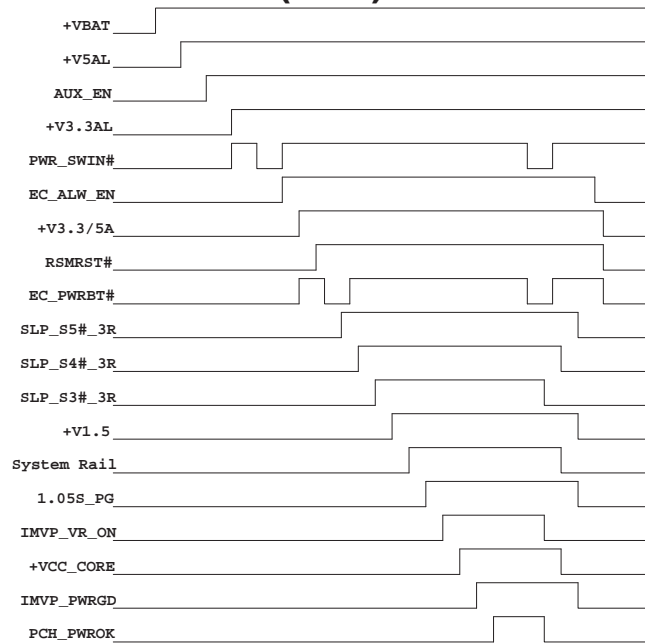
POWER SEQUENCY DIAGRAM



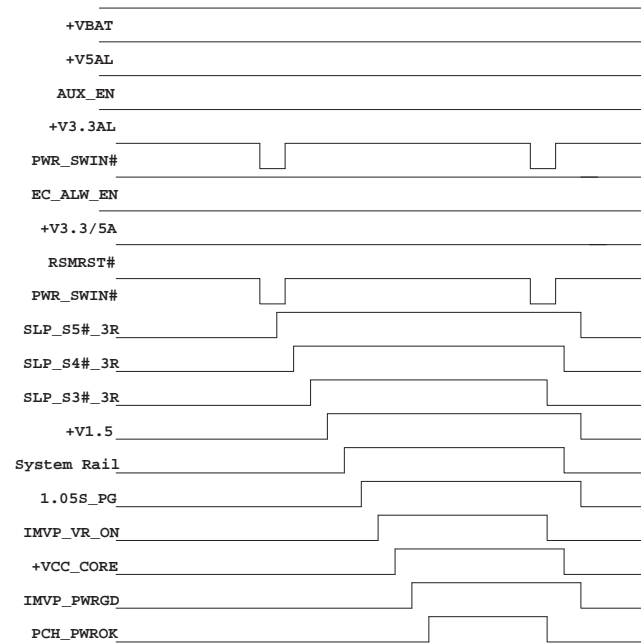
	Source Rail	EN	PG	Power Status				Remark
				S0	S3	AC S4/S5	DC S4/S5	
+VBAT				V	V	V	V	
+V5AL	+VBAT	+V3.3A_RTC		V	V	V	V	
+V3.3AL	+VBAT	+V5AL		V	V	V	V	
+V5A	+VBAT	EC_ALW_EN		V	V	V		
+V3.3A	+V3.3AL	EC_ALW_EN		V	V	V		
+V1.5	+VBAT	SLP_S4#_3R		V	V			
+V0.75S	+V1.5	VTT_PG		V				
+V1.5S	+V1.5	RUN_ON_LOAD		V				
+V1.5_VDDQ	+V1.5	RUN_ON_LOAD		V				
+VCC_CORE	+VBAT	IMVP_VR_ON	IMVP_PWRGD	V				
+VTT	+VBAT	SLP_S3#_3R	VTT_PG	V				
+VGFX_CORE	+VBAT	GFX_VR_EN		V				
+V1.8S	+VBAT	SLP_S3#_3R		V				
+V1.05S	+VBAT	SLP_S3#_3R	1.05S_PG	V				
+V5S	+V5A	RUN_ON_LOAD		V				
+V3.3S	+V3.3A	RUN_ON_LOAD		V				
+VDD_CORE	+VBAT	SLP_S3#_3R		V				
+V3.3S_Delay	+V3.3S	+V1.8S		V				
+VPCIE	+V1.5S	SLP_S3#_3R		V				

POWER SEQUENCE TIMING

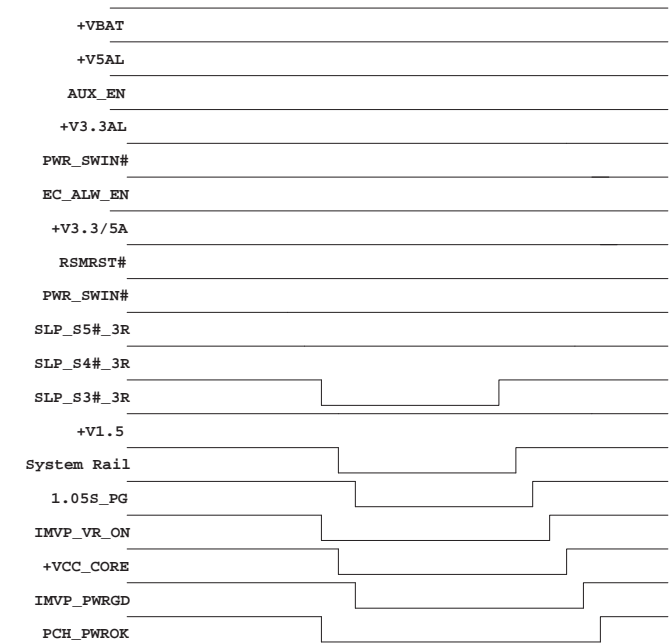
G3(OFF)->S0->S5



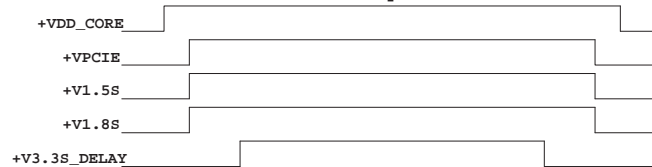
S5->S0->S5



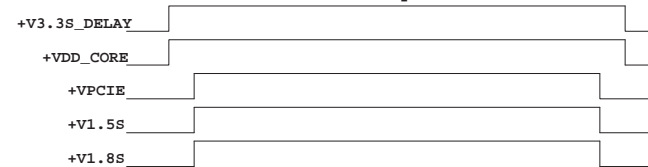
S0->S3->S0



M93 Sequence

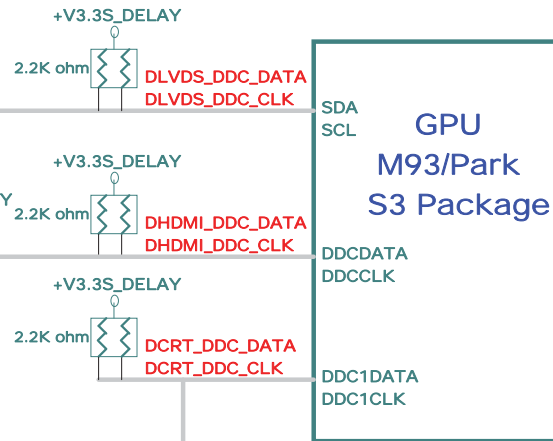


Park Sequence

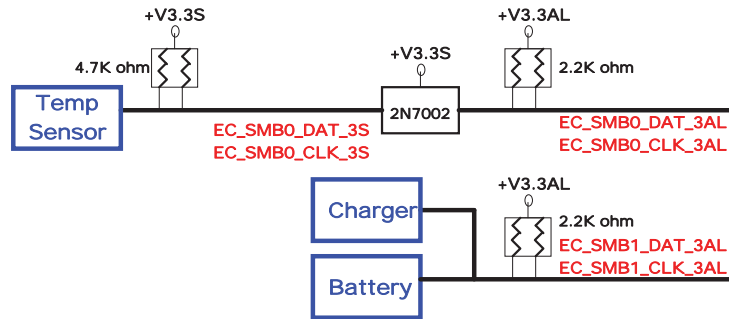
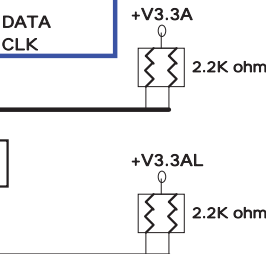
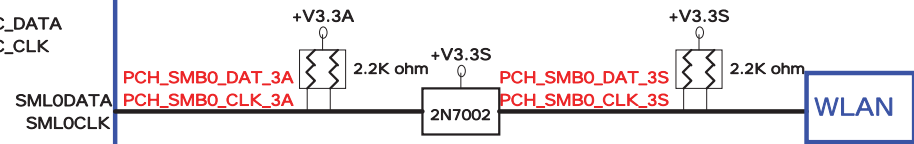
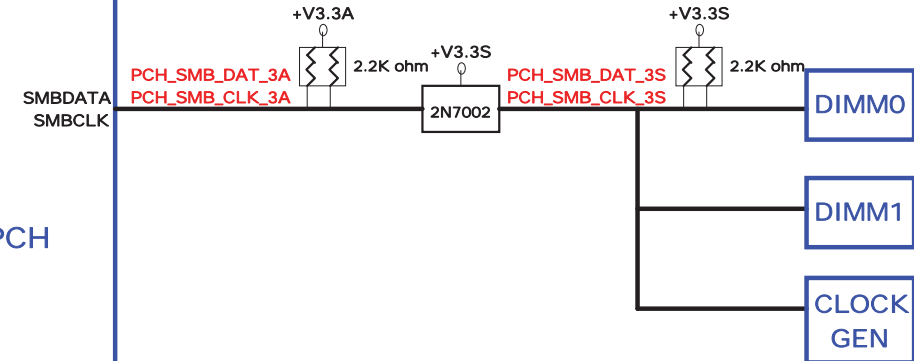


SMBUS&I2C MAP


Discrete
GPU



PCH

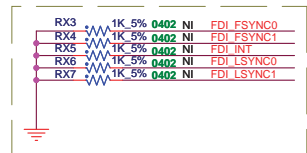


RESET SIGNAL MAP

		Hon Hai Precision Industry Co. Ltd.	
Foxconn eMS Inc.		HNBD R&D	
		phone: +886-2-2799-6111	
Title			
RESET SIGNAL MAP			
Size	Document Number		Rev
Custom	STAR (Federer)		0.4
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```
Discrete GPU: Install
UMA: Not Install
```




```
CFG4      Display Port Presence
CFG4      1 : Disabled ; No Physical Display Port
          attached to Embedded Display Port
          0 : Enable ; An external Display Poert device
          is connected to the Embedded Display Port
```

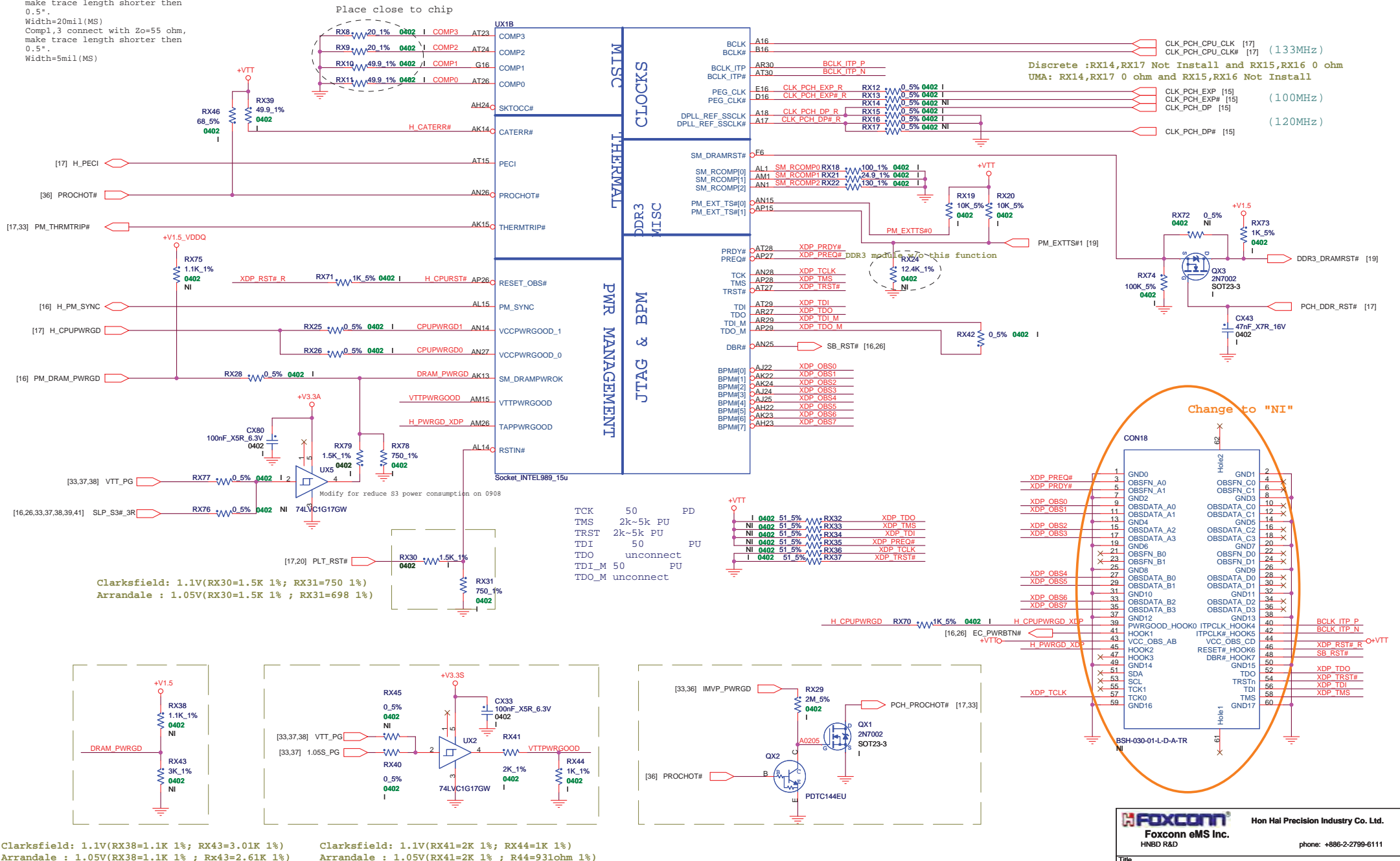
CFG7 Reserved - Temporarily used for early Clarksfield samples.
CFG7 Clarksfield (only for early samples pre-ES1) -
Connect to GND with 3.01K Ohm/5% resistor

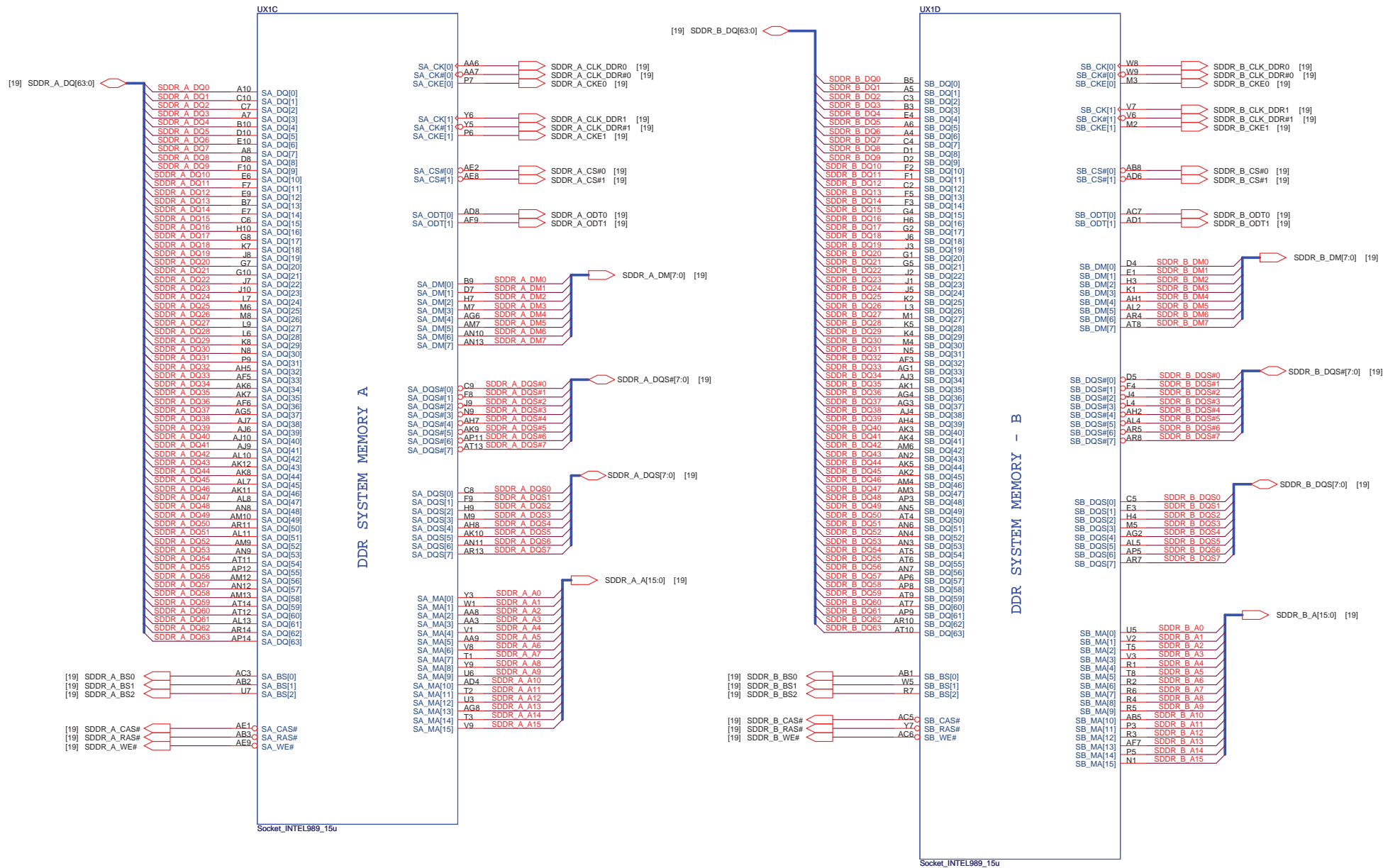
```
PCI Express Configuration Select
CFG0      1 : Single PEG
          0 : Bifurcation enabled
```

```
CFG3      PCI Express Static Lane Reversal
CFG3      1 : Normal Operation
          0 : Lane Numbers Reversed
           15 -> 0 , 14 -> 1 , ...
```

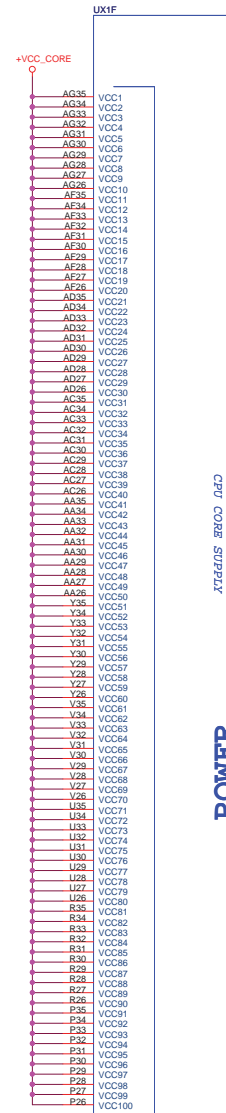
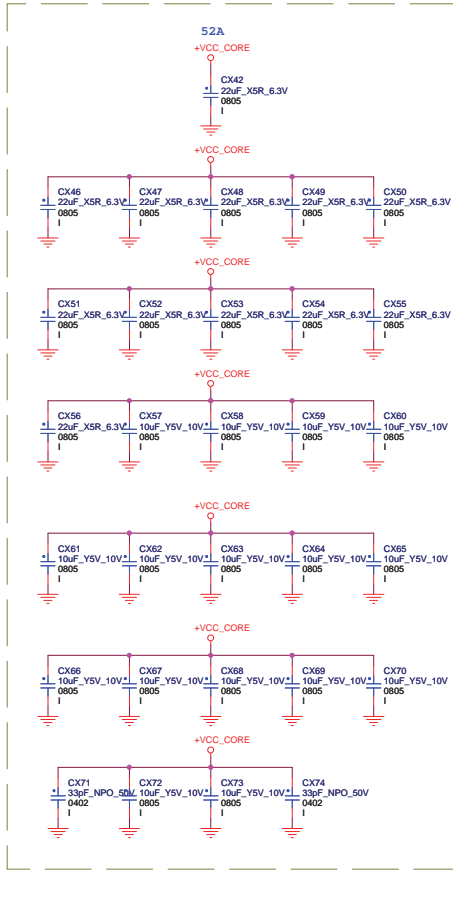
		Hon Hai Precision Industry Co. Ltd.	
Foxconn eMS Inc.		phone: +886-2-2799-6111	
HNBD R&D			
Title			
Calculla (DMI,PEG,FDI)			
Size	Document Number	Rev	
Custom	STAR (Federer)	0.4	
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Layout Note:
Comp0,2 connect with Zo=27.4 ohm,
make trace length shorter then
0.5".
Width=20mil(MS)
Comp1,3 connect with Zo=55 ohm,
make trace length shorter then
0.5".
Width=5mil(MS)





FOR VCC:
12x 0805 22 μ F inside cavity,
7x 0805 10 μ F under cavity and 9 x 0805 10 μ F
between inductor and socket on top layer



Socket_INTEL989_15u

CPU CORE STRIPLEX

POWER

CPU VIDS

SENSE

SENSE

SENSE

SENSE

SENSE

SENSE

SENSE

SENSE

SENSE

SENSE

SENSE

SENSE

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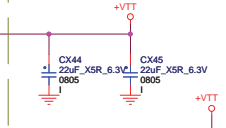
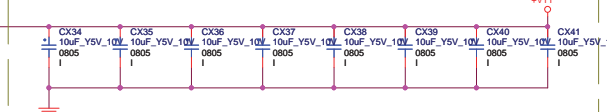
SENSE

SENSE

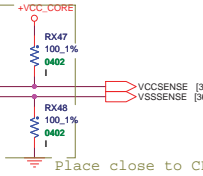
SENSE

SENSE

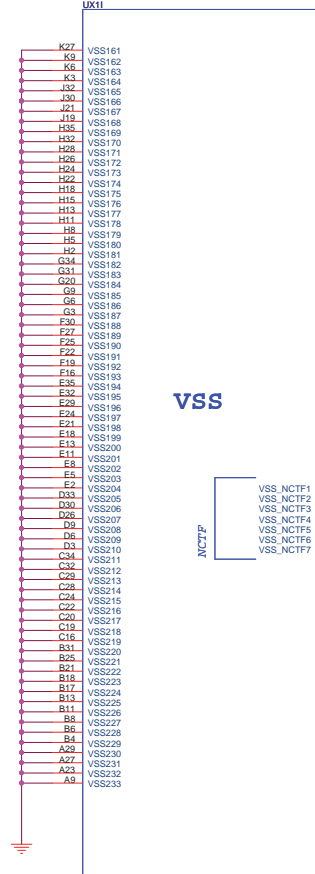
FOR VTT:
7x 0805 22 μ F under
cavity
8x 0805 10 μ F edge caps



Arrandale drives this pin High
Clarkfield drives this pin Low.



Place close to CPU



VSS

VSS

VSS

VSS

VSS

VSS

VSS

VSS

VSS

VSS

VSS

VSS

VSS

VSS

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VSS

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VSS

VSS

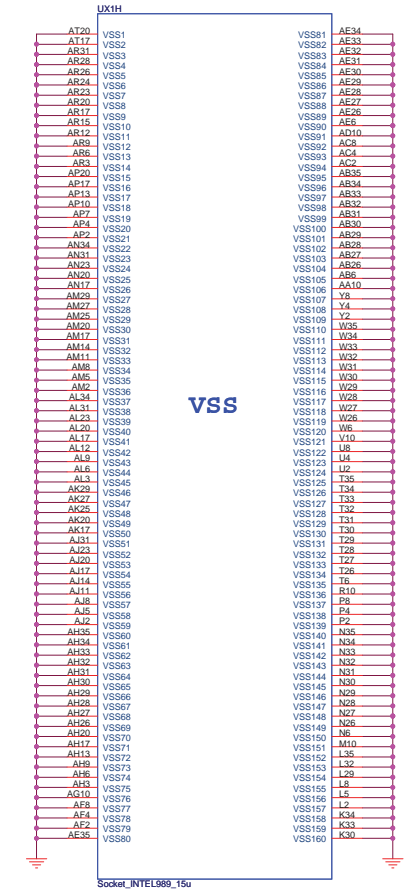
VSS

VSS

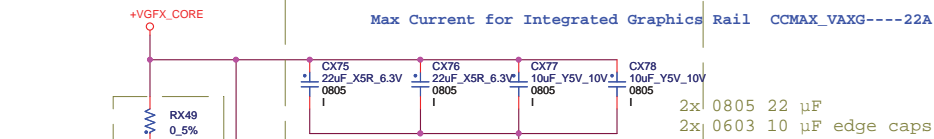
VSS

VSS

VSS



Socket_INTEL989_15u



Discrete GPU: Not Install
UMA: Install

GRAPHICS

POWER

SENSE LINES

GRAPHICS VIDS

DDR3 - 1.5V RAILS

1.1V

1.8V

FBG & IMT

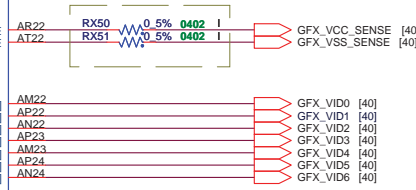
Socket_INTEL989_15u

+VTTQ [10,12,17,18,28,36,37,40]
+VGF_XCORE [40]
+V1.5_VDDQ [10,18,28,30,39]
+V1.8SQ [18,38,39]

Discrete GPU: Not Install
UMA: Install

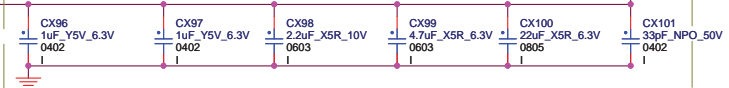
Discrete GPU: Install
UMA: Not Install

Discrete GPU: Not Install
UMA: Install

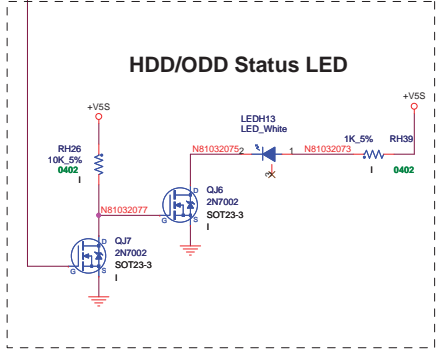
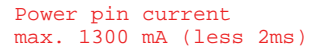


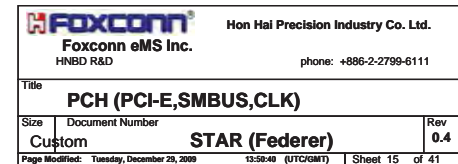
5x 0402 1 uF
2x 0805 22 uF

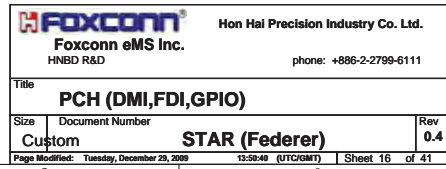
Max Current for VCCPLL Rail 1.35A



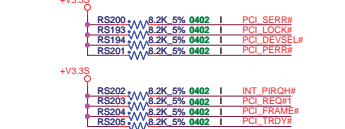
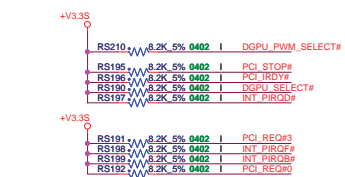
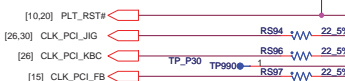
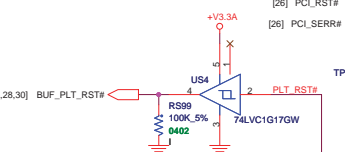
1x 0805 2.2 uF
2x 0805 1 uF
1x 0805 22 uF
1x 0603 4.7 uF







+V3.3A [10,14,15,16,18,26,28,30,33,34,38,39]
+V3.3S [10,14,15,16,18,19,20,26,27,28,29,30,31,32,33,36,37,38,39,40,41]
+VTT [10,12,13,18,28,36,37,40]

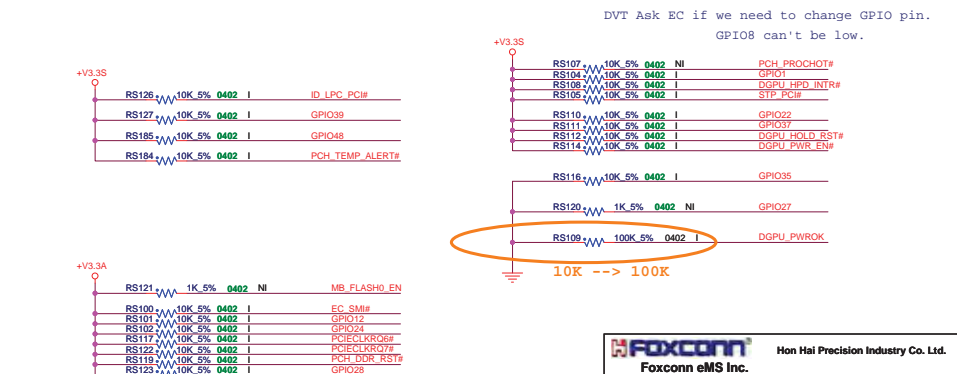
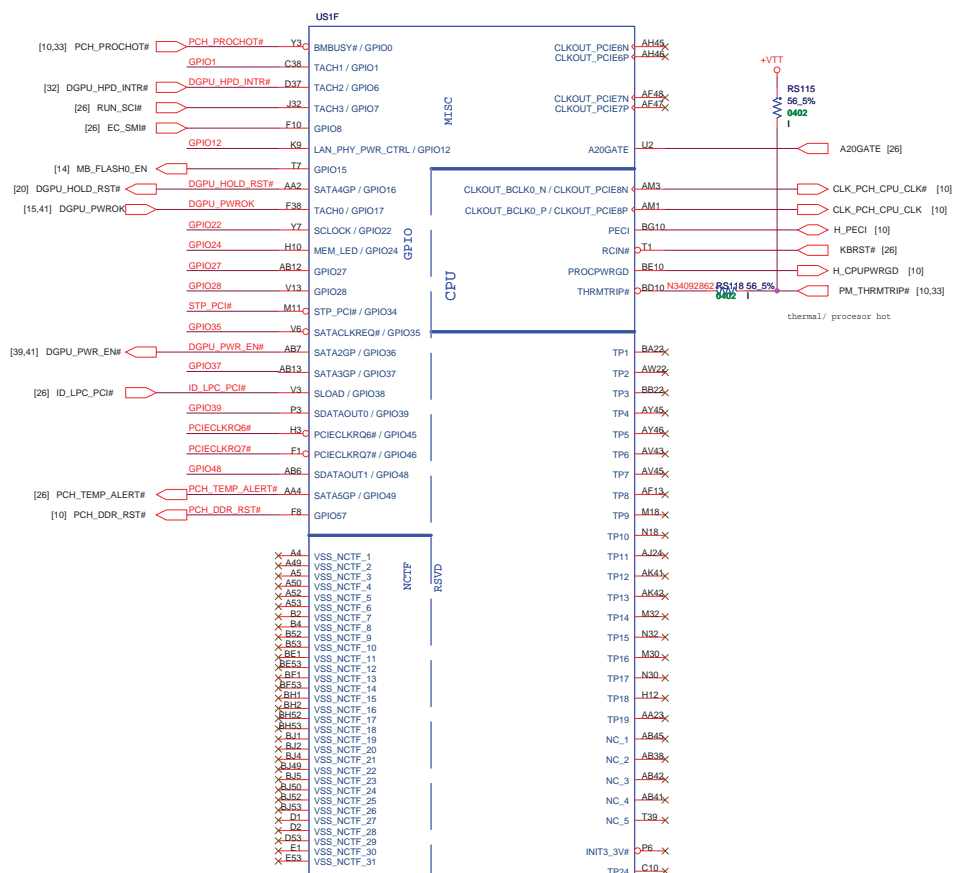


USB PORT	Function	OC pin
PORT-0	Ext. USB 0	
PORT-1	Ext. USB 1	
PORT-2	Ext. USB 2	
PORT-3		
PORT-4		
PORT-5		
PORT-6		
PORT-7		
PORT-8	Bluetooth	
PORT-9		
PORT-10	Camera	
PORT-11	WLAN/WiMAX	
PORT-12	Card reader	
PORT-13		



DMI Termination Voltage
Set to Vas when LOW
NV_CLE Set to Vcc when HIGH

Danbury Technology
Disabled when Low
Enabled when High



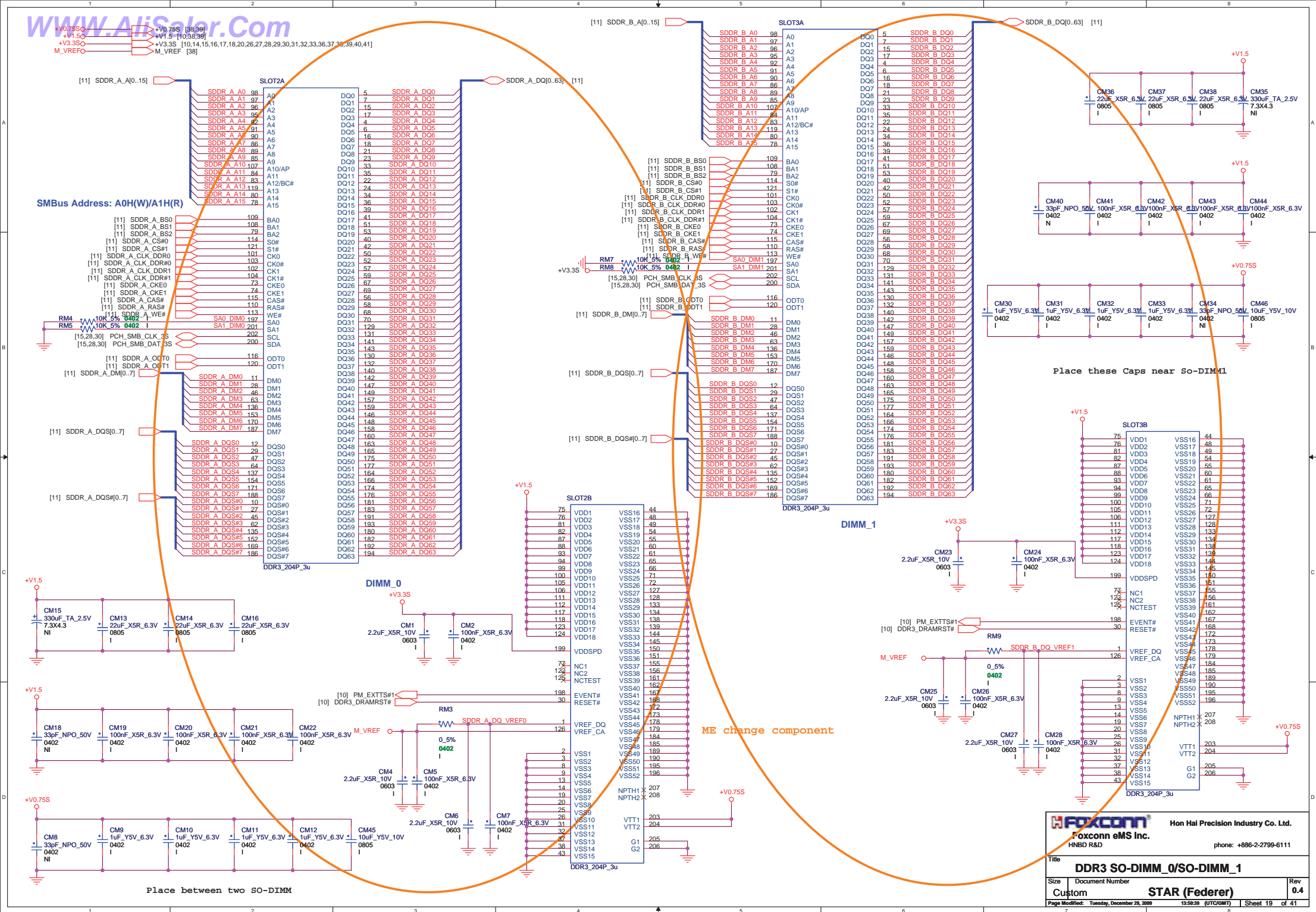
FOXCONN Hon Hai Precision Industry Co. Ltd.
Foxconn eMS Inc.
HNBID R&D
phone: +886-2-2799-6111

Tbno: **PCH (PCI,USB,NVRAM,GPIO)**

Size: Custom Document Number: **STAR (Federer)** Rev: 0.4

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Foxconn eMS Inc.
HNBD R&D phone: +886-2-2799-6111

Title: **DDR3 SO-DIMM_0/SO-DIMM_1**

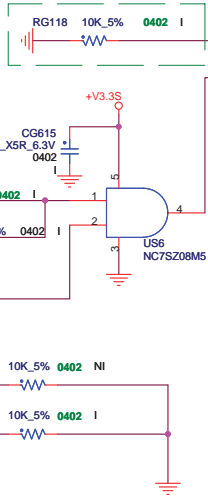
Size: Document Number

Custom: **STAR (Federer)**

Rev: **0.4**

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M93-S3 Not Install
PARK-S3 Install 10K ohm



If no ROM attached, GPIO[13:12:11] ;
CONFIG(2:0)
controls the memory aperture size.

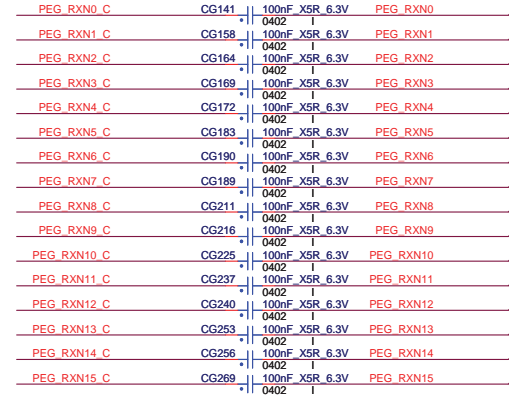
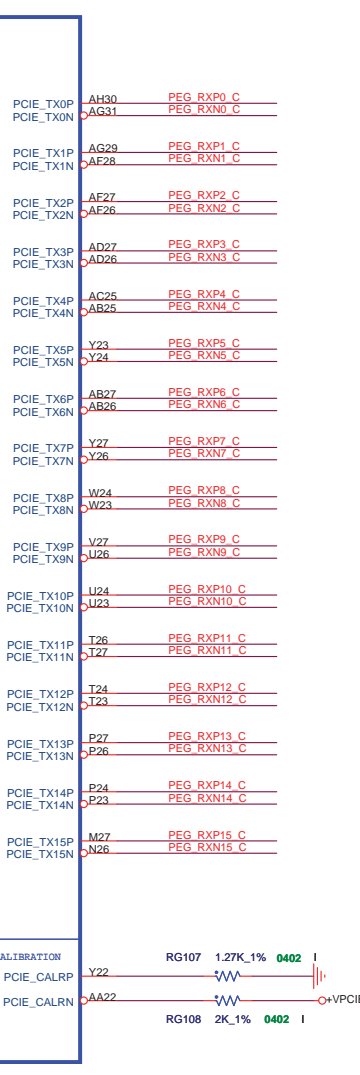
Reserved 011
512MB 001

HSYNC , VSYNC
AUD[1] , AUD[0]

0,0 No audio function
0,1 Audio for DisplayPort and HDMI if dongle is detected
1,0 Audio for DisplayPort only
1,1 Audio for both DisplayPort and HDMI

GPIO 0 : PCIE FULL TX OUTPUT SWING
GPIO 1 : PCIE TRANSMITTER DE-EMPHASIS ENABLED
GPIO 2 : PCIE GEN2 ENABLED

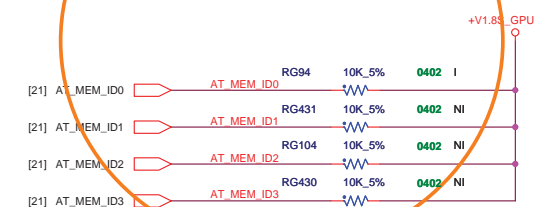
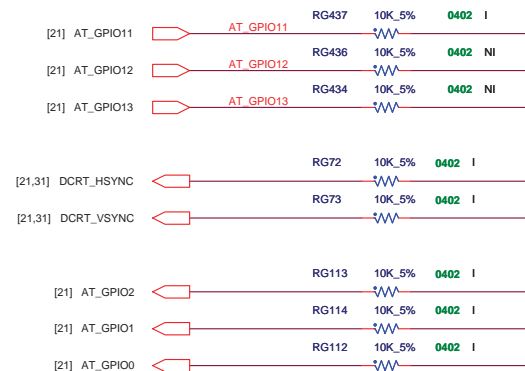
PCI EXPRESS INTERFACE



Modify setting by different VRAM vendor

Strap for DDR3
AT_MEM_ID (3:2:1:0)

0000	64Mx16	Samsung (K4W1G1646E-HC12)	512MB
0001	64Mx16	Hynix (H5TQ1G63BFR-12C)	512MB
0010	128Mx16	Samsung (K4W2G1646B-HC12)	1GB
0100	128Mx16	Samsung (K4W2G1646C-HCxx)	1GB
1000	128Mx16	Hynix (H5TQ2G63BFR-12C)	1GB
1001	128Mx16	Micron (MT41J128M16HA-12)	1GB



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Title
VGA (PCI-E/STRAP) 1/5

Size Document Number
Custom **STAR (Federer)**

Rev **0.4**

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+V3.3S_DELAY
+VPCIE
+V1.8S_GPU

M93-S3:Not Install
PARK-S3:Install

Del NorFlash parts

clock source change to clock gen.

UG268

M93-S3/M92-S2
DVCNTL_0 / DVPDATA_18
DVCNTL_1 / NC
DVCNTL_2 / TESTEN2
DVCNTL_12 / DVPDATA_18
DVCNTL_11 / DVPDATA_20
DVCNTL_10 / DVPDATA_22
DVCNTL_9 / DVPDATA_12
DVCNTL_8 / DVPDATA_14
DVCNTL_7 / DVPDATA_14
DVCNTL_6 / DVPDATA_14
DVCNTL_5 / DVPDATA_14
DVCNTL_4 / DVPDATA_4
DVCNTL_3 / DVPDATA_19
DVCNTL_2 / DVPDATA_21
DVCNTL_1 / DVPDATA_2
DVCNTL_0 / DVPDATA_0

M93-S3/M92-S2
DPC_PVDD / DVPDATA_11
DPC_PVSS / GND
DPC_VDD18H1 / DVPDATA10
DPC_VDD18H2 / DVPDATA13
DPC_VDD10H1 / DVPDATA15
DPC_VDD10H2 / DVPDATA17
DPC_VSSR1 / DVPCLK
DPC_VSSR2 / DVPDATA5
DPC_VSSR3 / GND
DPC_VSSR4 / GND
DPC_VSSR5 / DVPNTL_MV0
VDDR4 / DPCD_CALR

I2C

GENERAL PURPOSE I/O
GPIO_0
GPIO_1
GPIO_2
GPIO_3 / SMBDATA
GPIO_4 / SMBCLK
GPIO_5 / AC_BATT
GPIO_6
GPIO_7 / BLON
GPIO_8 / ROM50
GPIO_9 / ROMSI
GPIO_10 / ROMSK
GPIO_11
GPIO_12
GPIO_13
GPIO_14 / HPD2
GPIO_15 / PWRCNTL_0
GPIO_16 / SSN
GPIO_17 / THERMAL_INT
GPIO_18 / HPD3
GPIO_19 / HPD3
GPIO_20 / PWRCNTL_1
GPIO_21 / BB_EN
GPIO_22 / ROMCSB
GPIO_23 / CLKREQB

JTAG_TRSTB
JTAG_TDI
JTAG_TCK
JTAG_TMS
JTAG_TDO
TESTEN

GENERIC_A
GENERIC_B
GENERIC_C
GENERIC_D
GENERIC_HPDA

HPD1
VREFG

PLL_CLOCK
DPLL_PVDD
DPLL_PVSS
DPLL_VDDC
DPLL_VDDC

XTALIN
XTALOUT
NC2/XO_IN
NC1/XO_IN2

DPLL5
DPLL5

TS_FDO
TSVDD
TSVSS

Park_XT_S3

DPA
TXCAP_DPA3P
TXCAM_DPA3N
TXOP_DPA2P
TXOM_DPA2N
TX1P_DPA1P
TX1M_DPA1N
TX2P_DPA0P
TX2M_DPA0N
TXCBP_DPB3P
TXCBM_DPB3N
TX3P_DPB2P
TX3M_DPB2N
TX4P_DPB1P
TX4M_DPB1N
TX5P_DPB0P
TX5M_DPB0N

M92-S2/M93-S3
DVPDATA_3 / TXCCP_DPC3P
DVPNTL_2 / TXCCM_DPC3N
DVPDATA_7 / TXOP_DPC2P
DVPDATA_1 / TXOM_DPC2N
DVPNTL_MV1 / TX1P_DPC1P
DVPDATA_9 / TX1M_DPC1N
DVPDATA_13 / TX2P_DPC0P
DVPNTL_1 / TX2M_DPC0N
VDDR4 / DPCD_CALR

I2C

DAC1
R
RB
GB
BB
HSYNC
VSYNC
RSET
AVDD
AVSSQ
VDD1D1
VSS1D1
R2 / NC
R2B / NC
G2 / NC
G2B / NC
B2 / NC
B2B / NC
C / NC
Y / NC
COMP / NC

M92-S2/M93-S3
R2 / NC
R2B / NC
G2 / NC
G2B / NC
B2 / NC
B2B / NC
C / NC
Y / NC
COMP / NC

HSYNC
VSYNC
RSET
AVDD
AVSSQ
VDD1D1
VSS1D1
R2 / NC
R2B / NC
G2 / NC
G2B / NC
B2 / NC
B2B / NC
C / NC
Y / NC
COMP / NC

HPD1
VREFG

PLL_CLOCK
DPLL_PVDD
DPLL_PVSS
DPLL_VDDC
DPLL_VDDC

XTALIN
XTALOUT
NC2/XO_IN
NC1/XO_IN2

DPLL5
DPLL5

TS_FDO
TSVDD
TSVSS

Park_XT_S3

AF2
AF4
AG3
AG6
AH3
AH1
AK3
AK1
AK5
AK3
AK6
AK5
AJ7
AJ6
AK8
AK7

V4
V5
V3
V2
V4
V3
V4
V3
AA3
AA2
AA12

I2C

DAC2
R2 / NC
R2B / NC
G2 / NC
G2B / NC
B2 / NC
B2B / NC
C / NC
Y / NC
COMP / NC

M92-S2/M93-S3
R2 / NC
R2B / NC
G2 / NC
G2B / NC
B2 / NC
B2B / NC
C / NC
Y / NC
COMP / NC

HSYNC
VSYNC
RSET
AVDD
AVSSQ
VDD1D1
VSS1D1
R2 / NC
R2B / NC
G2 / NC
G2B / NC
B2 / NC
B2B / NC
C / NC
Y / NC
COMP / NC

HPD1
VREFG

PLL_CLOCK
DPLL_PVDD
DPLL_PVSS
DPLL_VDDC
DPLL_VDDC

XTALIN
XTALOUT
NC2/XO_IN
NC1/XO_IN2

DPLL5
DPLL5

TS_FDO
TSVDD
TSVSS

Park_XT_S3

TXCAP_DPA3P
TXCAM_DPA3N
TXOP_DPA2P
TXOM_DPA2N
TX1P_DPA1P
TX1M_DPA1N
TX2P_DPA0P
TX2M_DPA0N
TXCBP_DPB3P
TXCBM_DPB3N
TX3P_DPB2P
TX3M_DPB2N
TX4P_DPB1P
TX4M_DPB1N
TX5P_DPB0P
TX5M_DPB0N

M92-S2/M93-S3
DVPDATA_3 / TXCCP_DPC3P
DVPNTL_2 / TXCCM_DPC3N
DVPDATA_7 / TXOP_DPC2P
DVPDATA_1 / TXOM_DPC2N
DVPNTL_MV1 / TX1P_DPC1P
DVPDATA_9 / TX1M_DPC1N
DVPDATA_13 / TX2P_DPC0P
DVPNTL_1 / TX2M_DPC0N
VDDR4 / DPCD_CALR

I2C

DAC1
R
RB
GB
BB
HSYNC
VSYNC
RSET
AVDD
AVSSQ
VDD1D1
VSS1D1
R2 / NC
R2B / NC
G2 / NC
G2B / NC
B2 / NC
B2B / NC
C / NC
Y / NC
COMP / NC

M92-S2/M93-S3
R2 / NC
R2B / NC
G2 / NC
G2B / NC
B2 / NC
B2B / NC
C / NC
Y / NC
COMP / NC

HSYNC
VSYNC
RSET
AVDD
AVSSQ
VDD1D1
VSS1D1
R2 / NC
R2B / NC
G2 / NC
G2B / NC
B2 / NC
B2B / NC
C / NC
Y / NC
COMP / NC

HPD1
VREFG

PLL_CLOCK
DPLL_PVDD
DPLL_PVSS
DPLL_VDDC
DPLL_VDDC

XTALIN
XTALOUT
NC2/XO_IN
NC1/XO_IN2

DPLL5
DPLL5

TS_FDO
TSVDD
TSVSS

Park_XT_S3

AF2
AF4
AG3
AG6
AH3
AH1
AK3
AK1
AK5
AK3
AK6
AK5
AJ7
AJ6
AK8
AK7

V4
V5
V3
V2
V4
V3
V4
V3
AA3
AA2
AA12

I2C

DAC2
R2 / NC
R2B / NC
G2 / NC
G2B / NC
B2 / NC
B2B / NC
C / NC
Y / NC
COMP / NC

M92-S2/M93-S3
R2 / NC
R2B / NC
G2 / NC
G2B / NC
B2 / NC
B2B / NC
C / NC
Y / NC
COMP / NC

HSYNC
VSYNC
RSET
AVDD
AVSSQ
VDD1D1
VSS1D1
R2 / NC
R2B / NC
G2 / NC
G2B / NC
B2 / NC
B2B / NC
C / NC
Y / NC
COMP / NC

HPD1
VREFG

PLL_CLOCK
DPLL_PVDD
DPLL_PVSS
DPLL_VDDC
DPLL_VDDC

XTALIN
XTALOUT
NC2/XO_IN
NC1/XO_IN2

DPLL5
DPLL5

TS_FDO
TSVDD
TSVSS

Park_XT_S3

TXCAP_DPA3P
TXCAM_DPA3N
TXOP_DPA2P
TXOM_DPA2N
TX1P_DPA1P
TX1M_DPA1N
TX2P_DPA0P
TX2M_DPA0N
TXCBP_DPB3P
TXCBM_DPB3N
TX3P_DPB2P
TX3M_DPB2N
TX4P_DPB1P
TX4M_DPB1N
TX5P_DPB0P
TX5M_DPB0N

M92-S2/M93-S3
DVPDATA_3 / TXCCP_DPC3P
DVPNTL_2 / TXCCM_DPC3N
DVPDATA_7 / TXOP_DPC2P
DVPDATA_1 / TXOM_DPC2N
DVPNTL_MV1 / TX1P_DPC1P
DVPDATA_9 / TX1M_DPC1N
DVPDATA_13 / TX2P_DPC0P
DVPNTL_1 / TX2M_DPC0N
VDDR4 / DPCD_CALR

I2C

DAC1
R
RB
GB
BB
HSYNC
VSYNC
RSET
AVDD
AVSSQ
VDD1D1
VSS1D1
R2 / NC
R2B / NC
G2 / NC
G2B / NC
B2 / NC
B2B / NC
C / NC
Y / NC
COMP / NC

M92-S2/M93-S3
R2 / NC
R2B / NC
G2 / NC
G2B / NC
B2 / NC
B2B / NC
C / NC
Y / NC
COMP / NC

HSYNC
VSYNC
RSET
AVDD
AVSSQ
VDD1D1
VSS1D1
R2 / NC
R2B / NC
G2 / NC
G2B / NC
B2 / NC
B2B / NC
C / NC
Y / NC
COMP / NC

HPD1
VREFG

PLL_CLOCK
DPLL_PVDD
DPLL_PVSS
DPLL_VDDC
DPLL_VDDC

XTALIN
XTALOUT
NC2/XO_IN
NC1/XO_IN2

DPLL5
DPLL5

TS_FDO
TSVDD
TSVSS

Park_XT_S3

AF2
AF4
AG3
AG6
AH3
AH1
AK3
AK1
AK5
AK3
AK6
AK5
AJ7
AJ6
AK8
AK7

V4
V5
V3
V2
V4
V3
V4
V3
AA3
AA2
AA12

I2C

DAC2
R2 / NC
R2B / NC
G2 / NC
G2B / NC
B2 / NC
B2B / NC
C / NC
Y / NC
COMP / NC

M92-S2/M93-S3
R2 / NC
R2B / NC
G2 / NC
G2B / NC
B2 / NC
B2B / NC
C / NC
Y / NC
COMP / NC

HSYNC
VSYNC
RSET
AVDD
AVSSQ
VDD1D1
VSS1D1
R2 / NC
R2B / NC
G2 / NC
G2B / NC
B2 / NC
B2B / NC
C / NC
Y / NC
COMP / NC

HPD1
VREFG

PLL_CLOCK
DPLL_PVDD
DPLL_PVSS
DPLL_VDDC
DPLL_VDDC

XTALIN
XTALOUT
NC2/XO_IN
NC1/XO_IN2

DPLL5
DPLL5

TS_FDO
TSVDD
TSVSS

Park_XT_S3

TXCAP_DPA3P
TXCAM_DPA3N
TXOP_DPA2P
TXOM_DPA2N
TX1P_DPA1P
TX1M_DPA1N
TX2P_DPA0P
TX2M_DPA0N
TXCBP_DPB3P
TXCBM_DPB3N
TX3P_DPB2P
TX3M_DPB2N
TX4P_DPB1P
TX4M_DPB1N
TX5P_DPB0P
TX5M_DPB0N

M92-S2/M93-S3
DVPDATA_3 / TXCCP_DPC3P
DVPNTL_2 / TXCCM_DPC3N
DVPDATA_7 / TXOP_DPC2P
DVPDATA_1 / TXOM_DPC2N
DVPNTL_MV1 / TX1P_DPC1P
DVPDATA_9 / TX1M_DPC1N
DVPDATA_13 / TX2P_DPC0P
DVPNTL_1 / TX2M_DPC0N
VDDR4 / DPCD_CALR

I2C

DAC1
R
RB
GB
BB
HSYNC
VSYNC
RSET
AVDD
AVSSQ
VDD1D1
VSS1D1
R2 / NC
R2B / NC
G2 / NC
G2B / NC
B2 / NC
B2B / NC
C / NC
Y / NC
COMP / NC

M92-S2/M93-S3
R2 / NC
R2B / NC
G2 / NC
G2B / NC
B2 / NC
B2B / NC
C / NC
Y / NC
COMP / NC

HSYNC
VSYNC
RSET
AVDD
AVSSQ
VDD1D1
VSS1D1
R2 / NC
R2B / NC
G2 / NC
G2B / NC
B2 / NC
B2B / NC
C / NC
Y / NC
COMP / NC

HPD1
VREFG

PLL_CLOCK
DPLL_PVDD
DPLL_PVSS
DPLL_VDDC
DPLL_VDDC

XTALIN
XTALOUT
NC2/XO_IN
NC1/XO_IN2

DPLL5
DPLL5

TS_FDO
TSVDD
TSVSS

Park_XT_S3

AF2
AF4
AG3
AG6
AH3
AH1
AK3
AK1
AK5
AK3
AK6
AK5
AJ7
AJ6
AK8
AK7

V4
V5
V3
V2
V4
V3
V4
V3
AA3
AA2
AA12

I2C

DAC2
R2 / NC
R2B / NC
G2 / NC
G2B / NC
B2 / NC
B2B / NC
C / NC
Y / NC
COMP / NC

M92-S2/M93-S3
R2 / NC
R2B / NC
G2 / NC
G2B / NC
B2 / NC
B2B / NC
C / NC
Y / NC
COMP / NC

HSYNC
VSYNC
RSET
AVDD
AVSSQ
VDD1D1
VSS1D1
R2 / NC
R2B / NC
G2 / NC
G2B / NC
B2 / NC
B2B / NC
C / NC
Y / NC
COMP / NC

HPD1
VREFG

PLL_CLOCK
DPLL_PVDD
DPLL_PVSS
DPLL_VDDC
DPLL_VDDC

XTALIN
XTALOUT
NC2/XO_IN
NC1/XO_IN2

DPLL5
DPLL5

TS_FDO
TSVDD
TSVSS

Park_XT_S3

AF2
AF4
AG3
AG6
AH3
AH1
AK3
AK1
AK5
AK3
AK6
AK5
AJ7
AJ6
AK8
AK7

V4
V5
V3
V2
V4
V3
V4
V3
AA3
AA2
AA12

I2C

DAC1
R
RB
GB
BB
HSYNC
VSYNC
RSET
AVDD
AVSSQ
VDD1D1
VSS1D1
R2 / NC
R2B / NC
G2 / NC
G2B / NC
B2 / NC
B2B / NC
C / NC
Y / NC
COMP / NC

M92-S2/M93-S3
R2 / NC
R2B / NC
G2 / NC
G2B / NC
B2 / NC
B2B / NC
C / NC
Y / NC
COMP / NC

HSYNC
VSYNC
RSET
AVDD
AVSSQ
VDD1D1
VSS1D1
R2 / NC
R2B / NC
G2 / NC
G2B / NC
B2 / NC
B2B / NC
C / NC
Y / NC
COMP / NC

HPD1
VREFG

PLL_CLOCK
DPLL_PVDD
DPLL_PVSS
DPLL_VDDC
DPLL_VDDC

XTALIN
XTALOUT
NC2/XO_IN
NC1/XO_IN2

DPLL5
DPLL5

TS_FDO
TSVDD
TSVSS

Park_XT_S3

AF2
AF4
AG3
AG6
AH3
AH1
AK3
AK1
AK5
AK3
AK6
AK5
AJ7
AJ6
AK8
AK7

V4
V5
V3
V2
V4
V3
V4
V3
AA3
AA2
AA12

I2C

DAC2
R2 / NC
R2B / NC
G2 / NC
G2B / NC
B2 / NC
B2B / NC
C / NC
Y / NC
COMP / NC

M92-S2/M93-S3
R2 / NC
R2B / NC
G2 / NC
G2B / NC
B2 / NC
B2B / NC
C / NC
Y / NC
COMP / NC

HSYNC
VSYNC
RSET
AVDD
AVSSQ
VDD1D1
VSS1D1
R2 / NC
R2B / NC
G2 / NC
G2B / NC
B2 / NC
B2B / NC
C / NC
Y / NC
COMP / NC

HPD1
VREFG

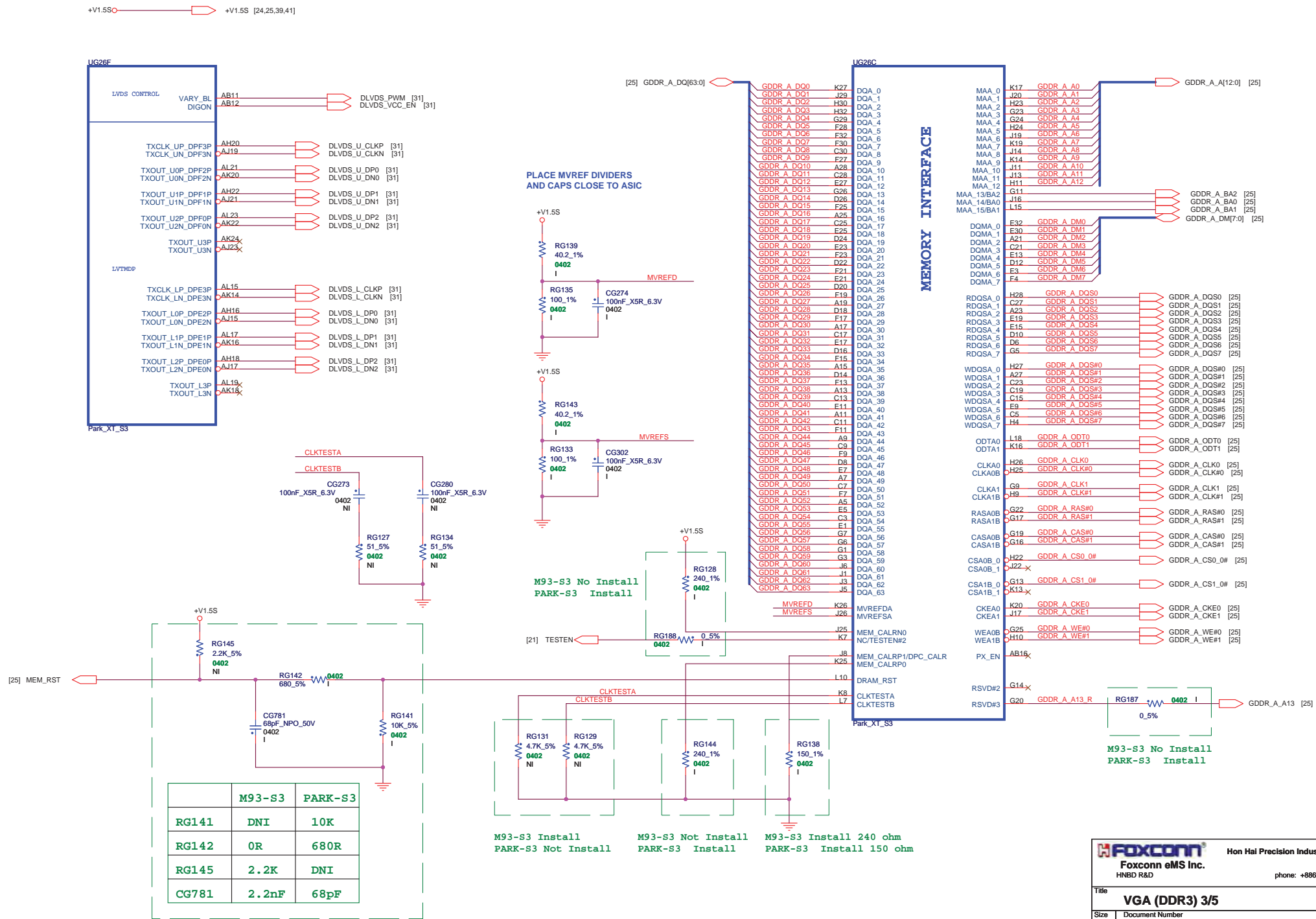
PLL_CLOCK
DPLL_PVDD
DPLL_PVSS
DPLL_VDDC
DPLL_VDDC

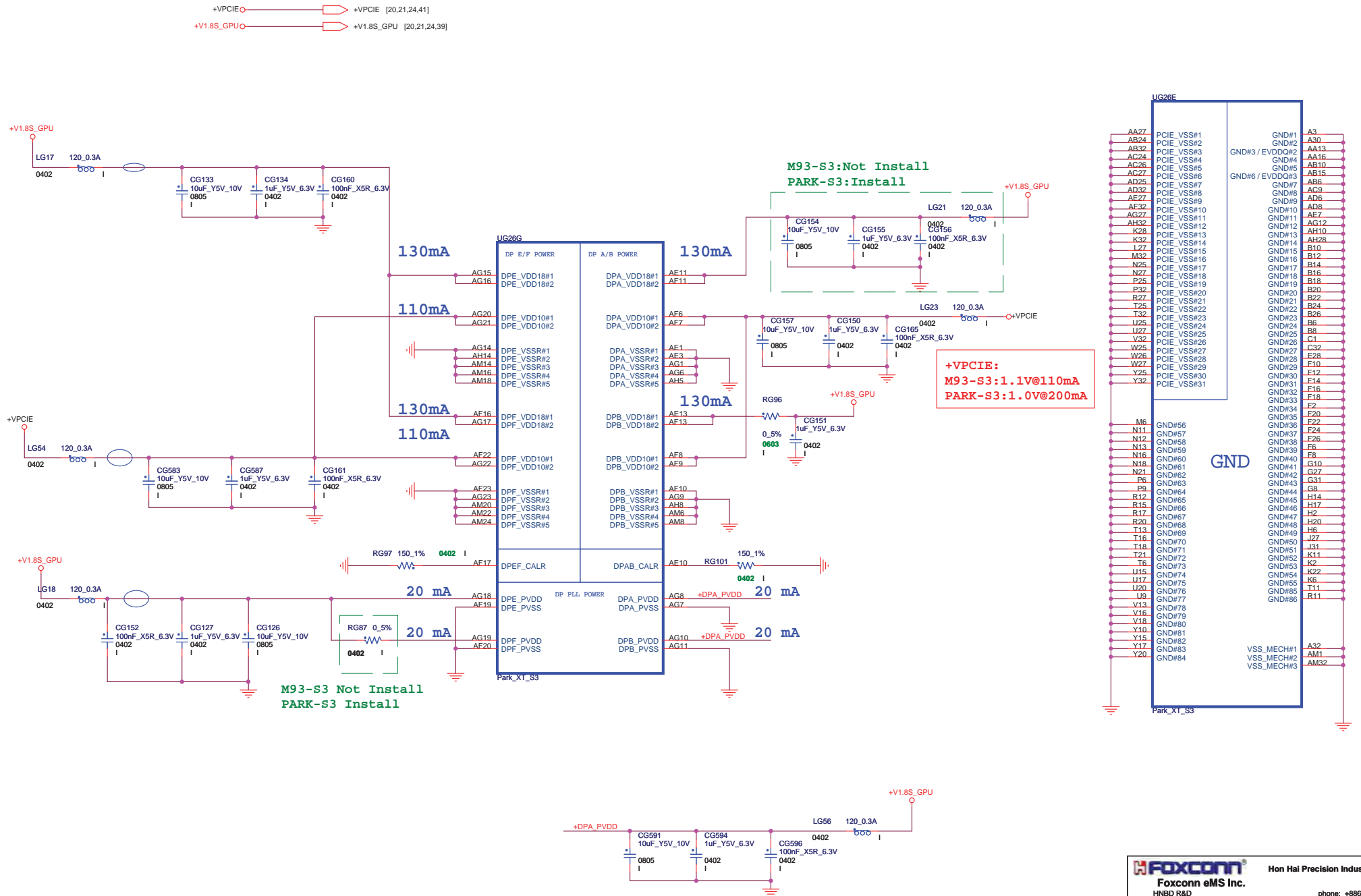
XTALIN
XTALOUT
NC2/XO_IN
NC1/XO_IN2

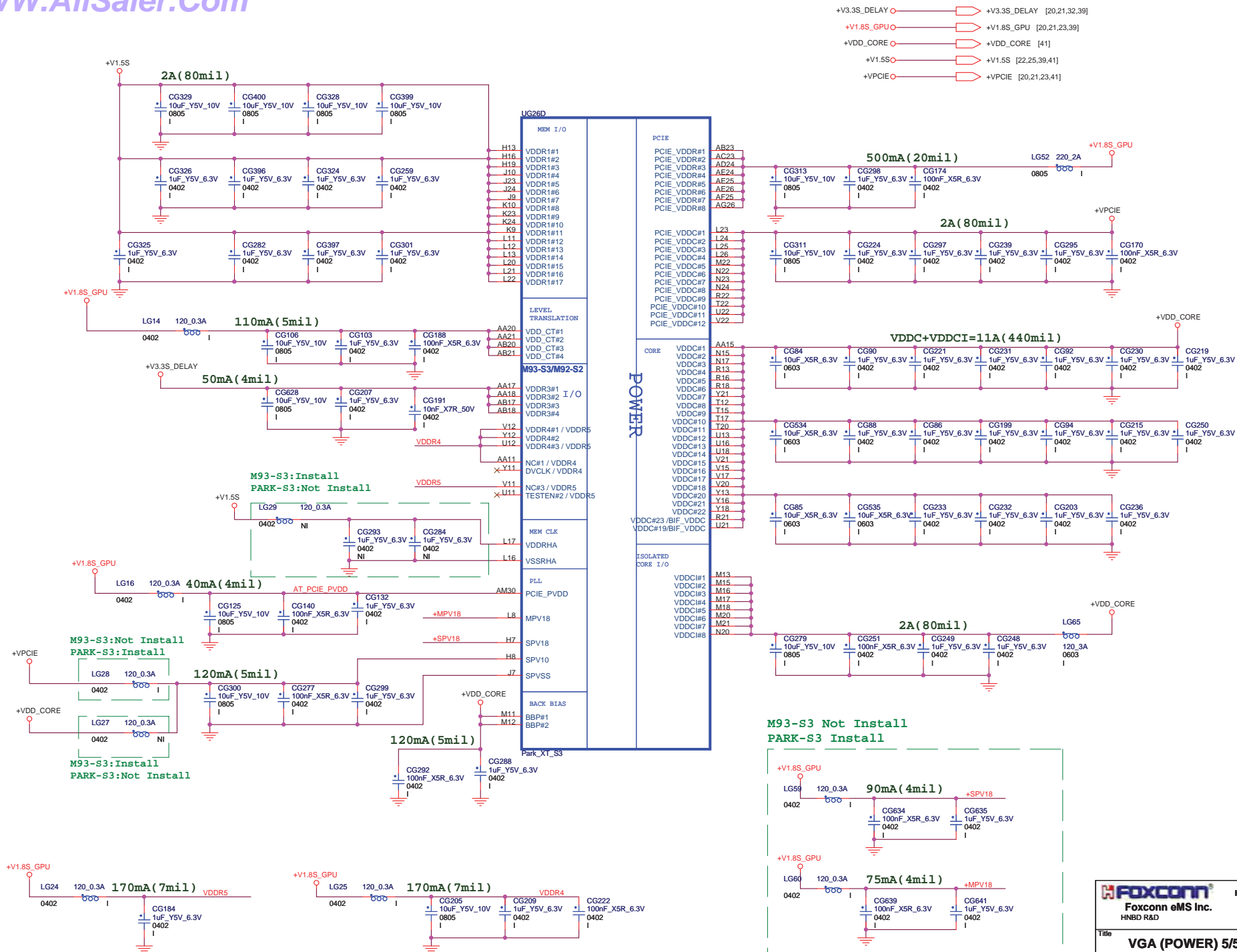
DPLL5
DPLL5

TS_FDO
TSVDD
TSVSS

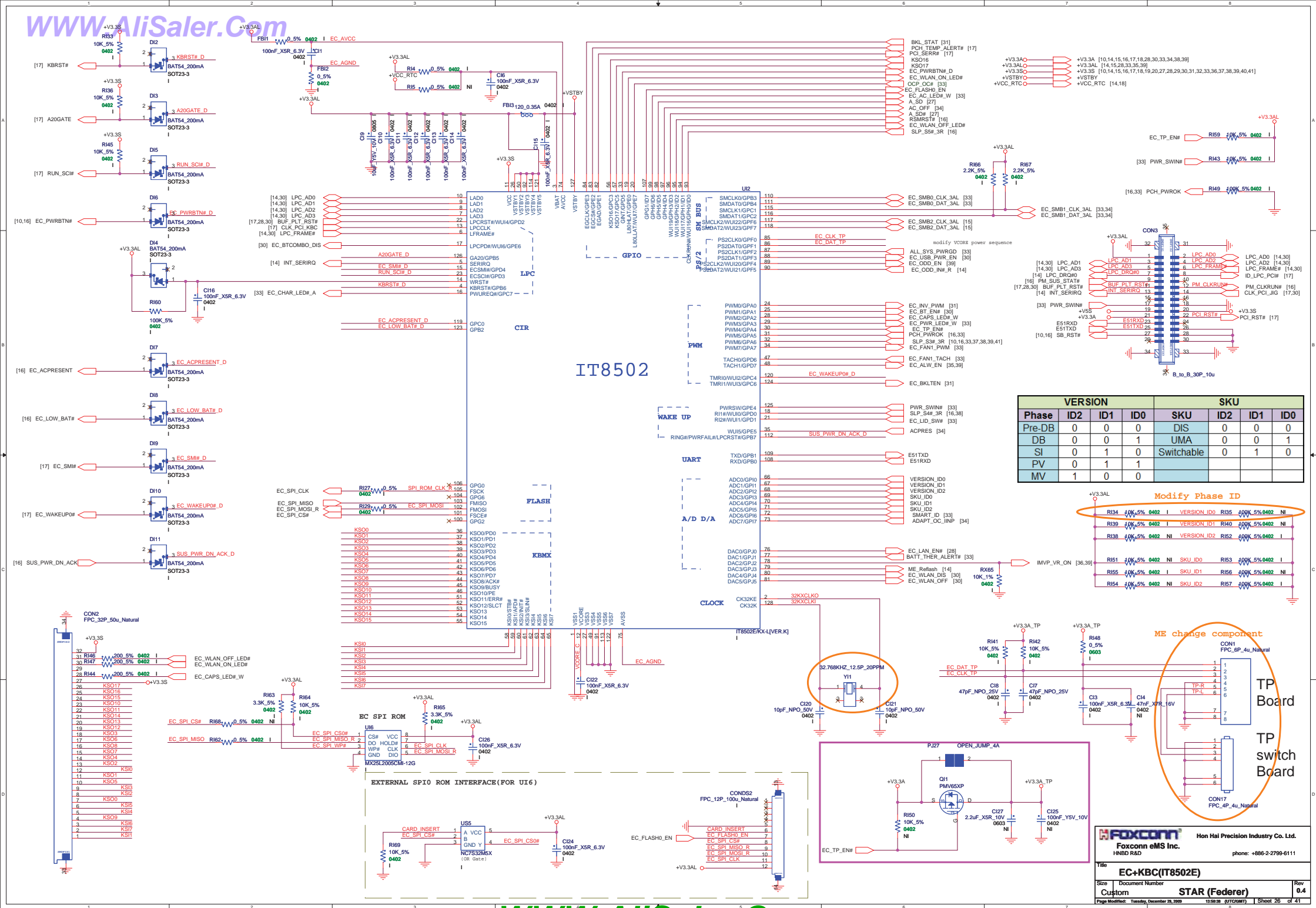
Park_XT_S3



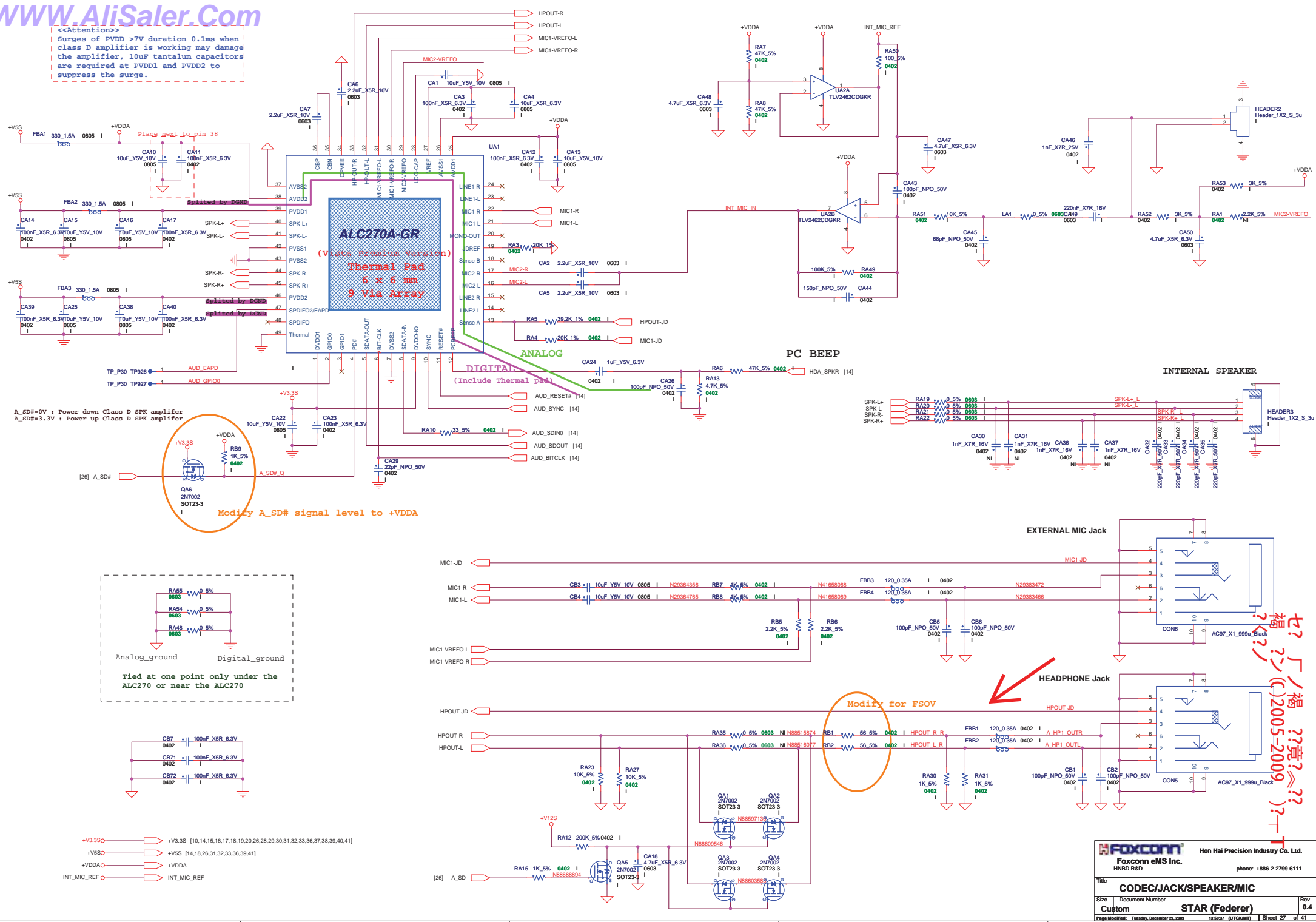


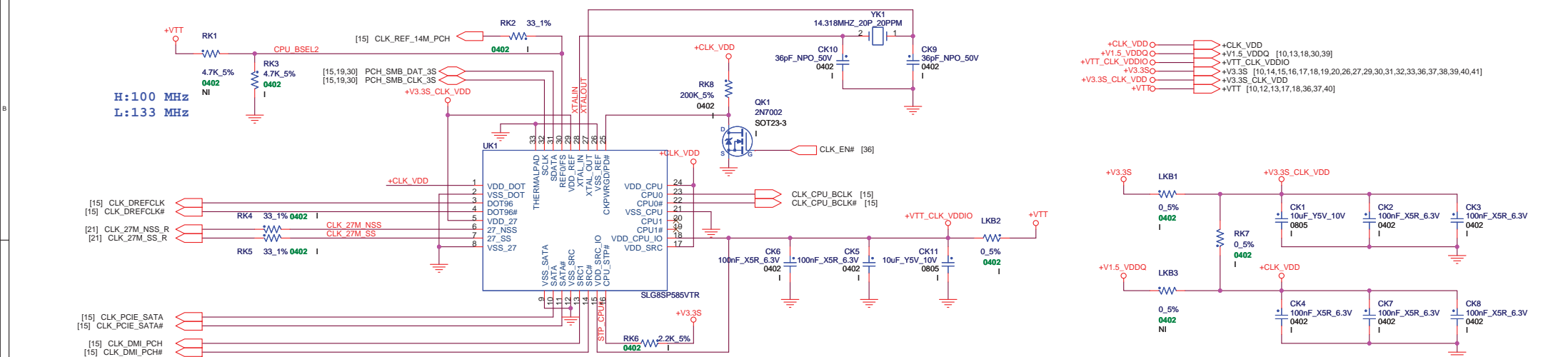
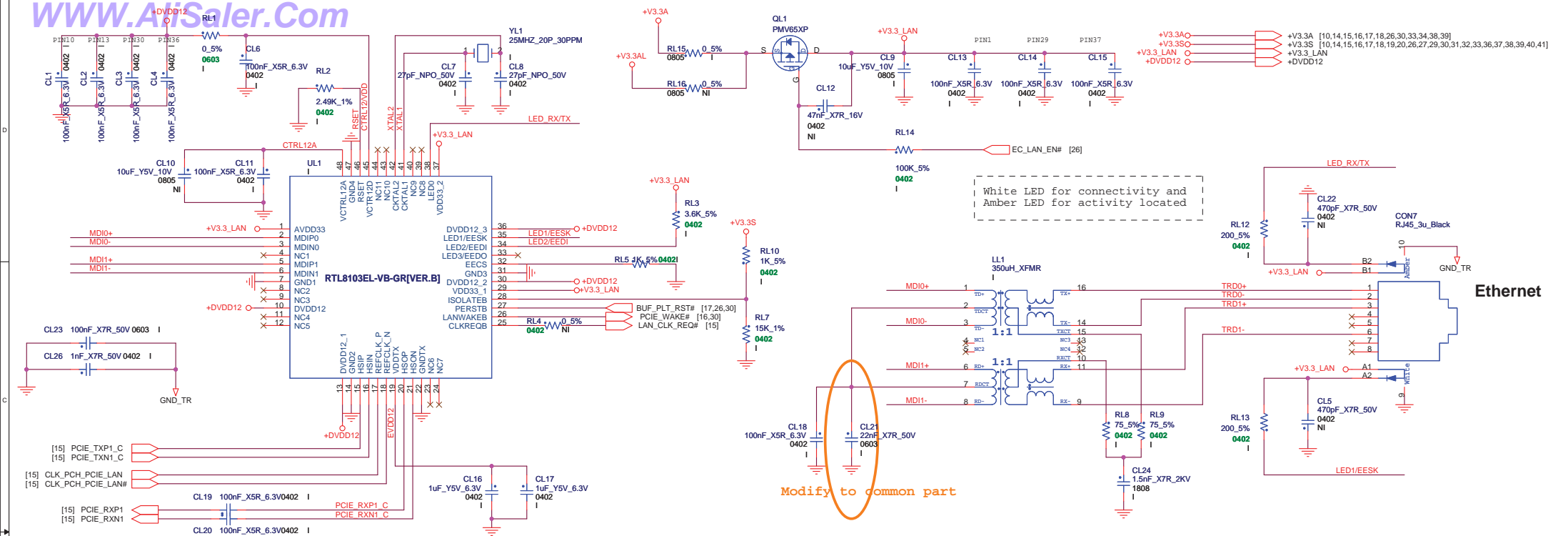







<<Attention>>
Surges of PVDD >7V duration 0.1ms when class D amplifier is working may damage the amplifier, 10uF tantalum capacitors are required at PVDD1 and PVDD2 to suppress the surge.

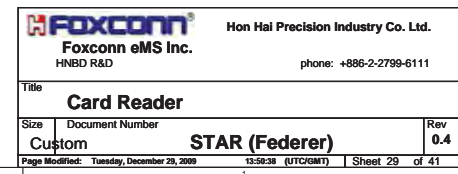


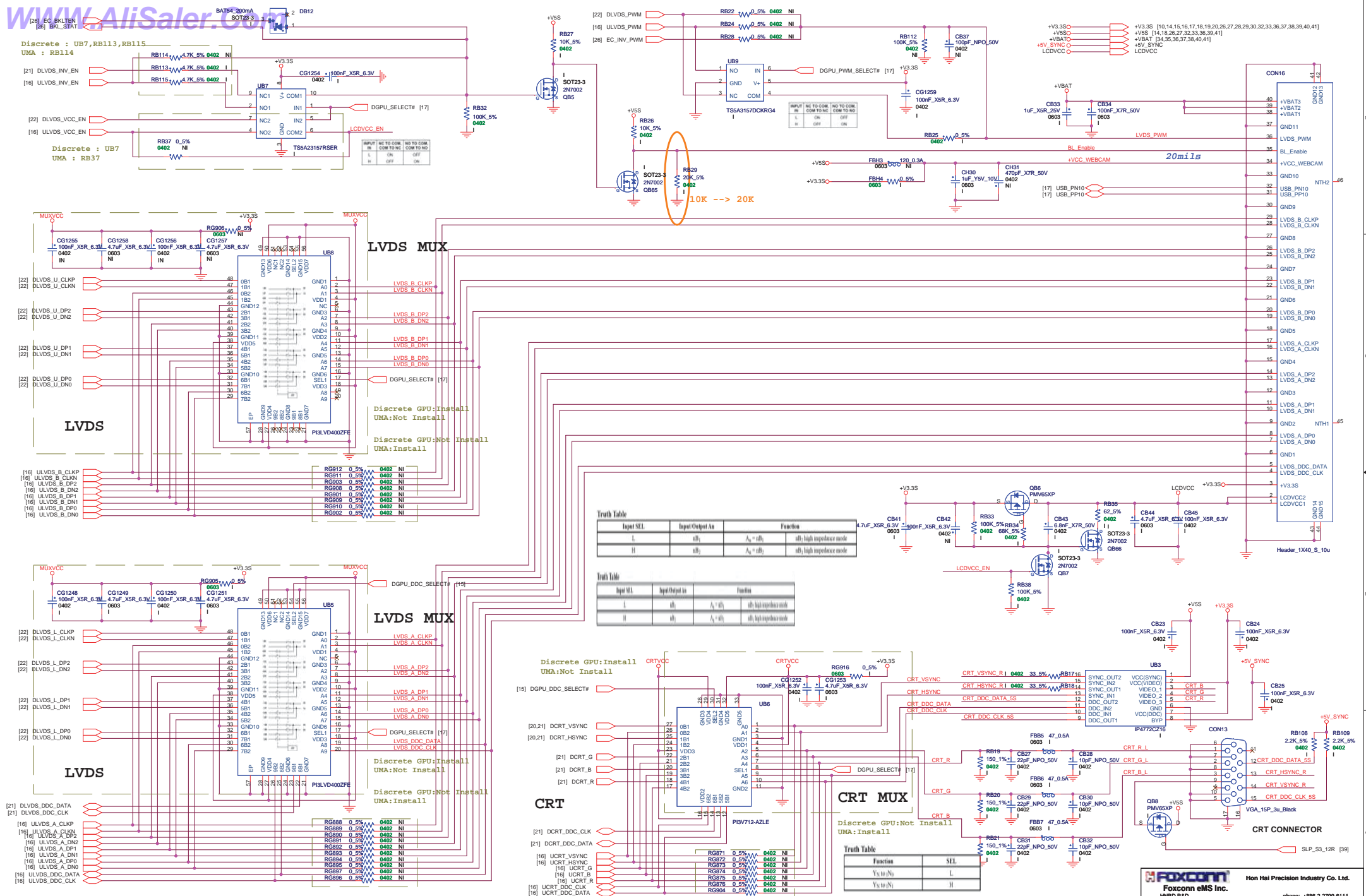


FSP Table

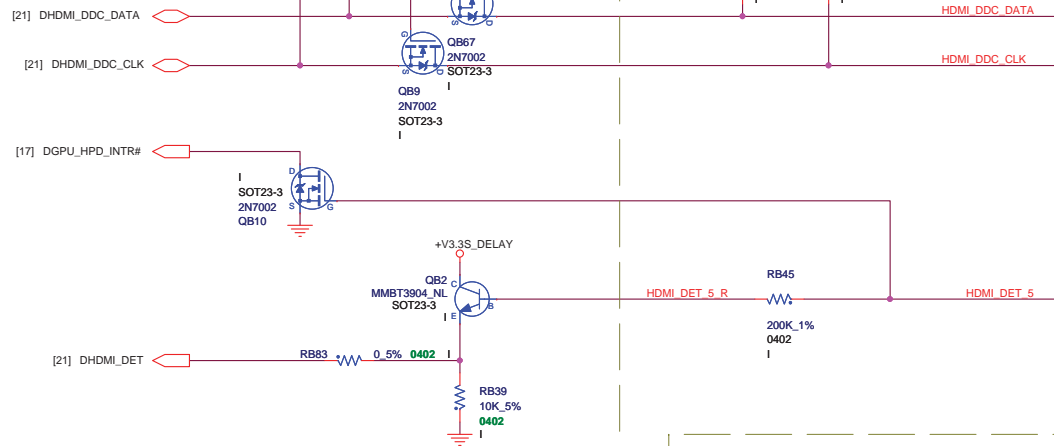
FS	CPU (PCH-->CPU)	Power On	SRC(DMI) (PCH-->CPU)	SATA (PCH)	DOT96 (PCH)	27MHz (GPU)	REF
0	133MHz	Default	100MHz	100MHz	96MHz	27MHz	14.318MHz
1	100MHz						

		Hon Hai Precision Industry Co. Ltd.	
Foxconn eMS Inc. HNBD R&D		phone: +886-2-2799-6111	
Title			
LAN (RTL8103EL)/CLOCK GEN			
Size	Document Number		Rev
Custom	STAR (Federer)		0.4
Page Modified: Tuesday, December 26, 2009		13:50:49 (UTC/GMT)	Sheet 28 of 41

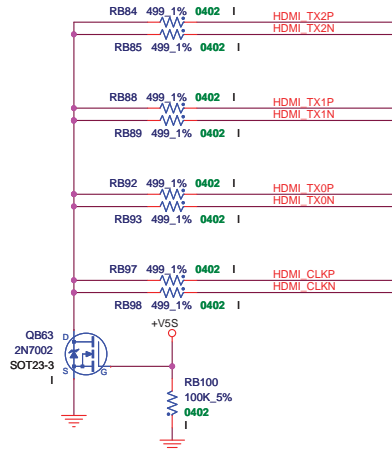




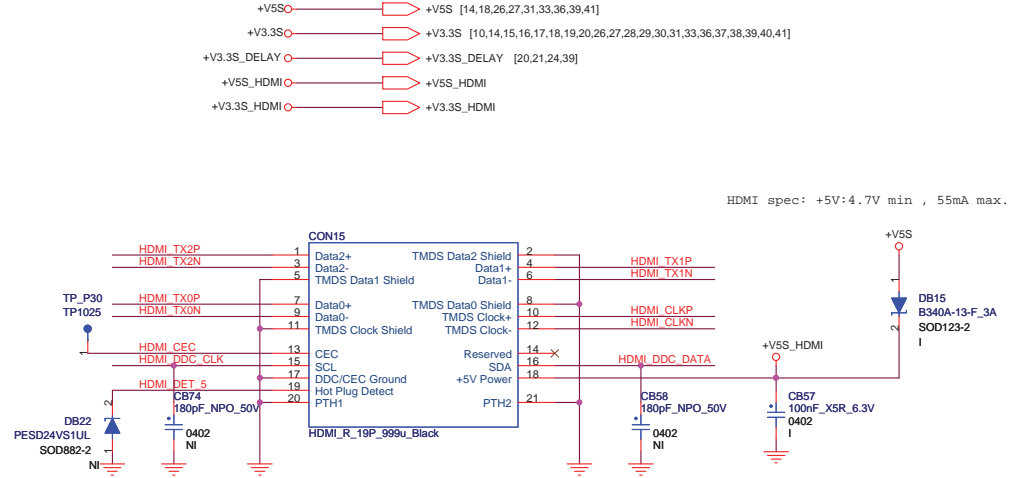
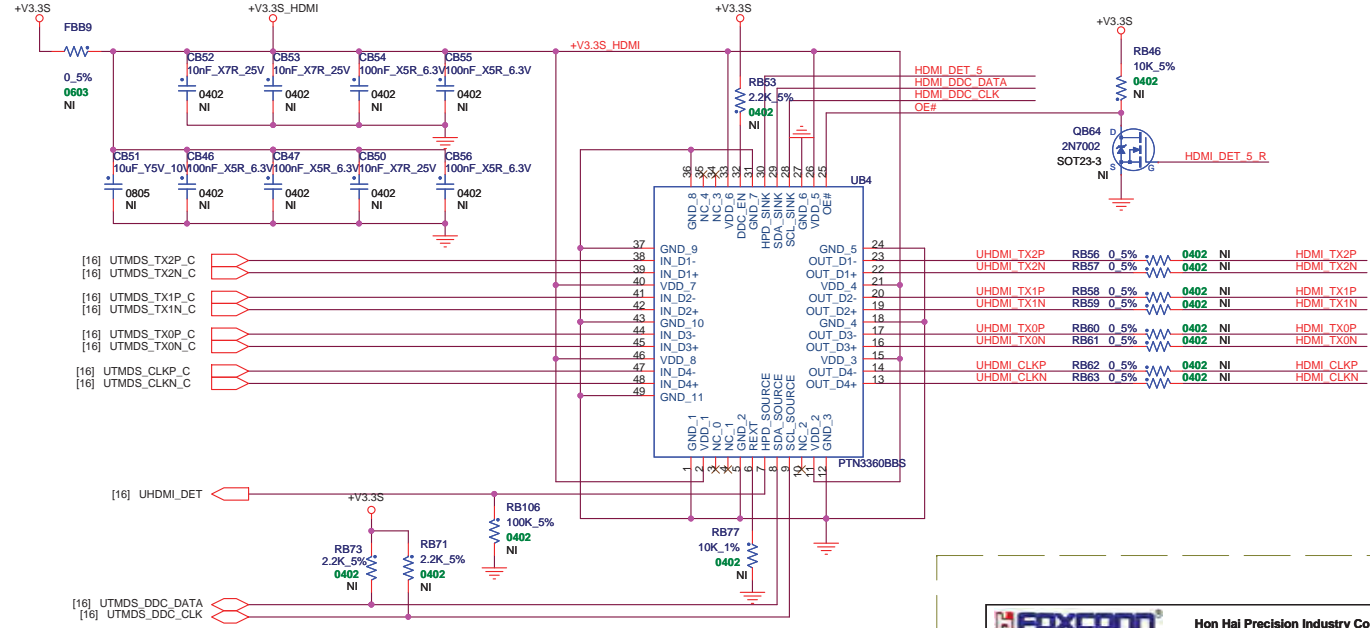
Discrete GPU: Install
UMA: Not Install



[21] DHDMI_TX2P	CB63 0402	100nF X5R 6.3V	I	HDMI TX2P
[21] DHDMI_TX2N	CB64 0402	100nF X5R 6.3V	I	HDMI TX2N
[21] DHDMI_TX1P	CB65 0402	100nF X5R 6.3V	I	HDMI TX1P
[21] DHDMI_TX1N	CB66 0402	100nF X5R 6.3V	I	HDMI TX1N
[21] DHDMI_TX0P	CB67 0402	100nF X5R 6.3V	I	HDMI TX0P
[21] DHDMI_TX0N	CB68 0402	100nF X5R 6.3V	I	HDMI TX0N
[21] DHDMI_CLKP	CB69 0402	100nF X5R 6.3V	I	HDMI CLKP
[21] DHDMI_CLKN	CB70 0402	100nF X5R 6.3V	I	HDMI CLKN



Discrete GPU:Not Install
UMA:Install

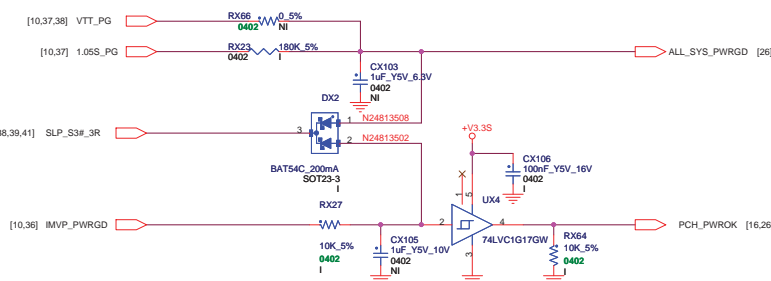


FAN CONNECTOR



DC_JACK
Wire to Board

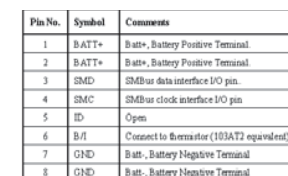
BT+ [34]
DCIN [34]
+V3.3AL [14,15,26,28,35,39]
+V3.3A [10,14,15,16,17,18,26,28,30,34,38,39]
+V3.3S [10,14,15,16,17,18,19,20,26,27,28,29,30,31,32,36,37,38,39,40,41]
M31ALDOO [34]




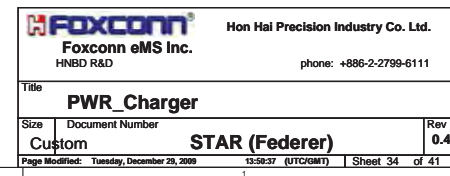
THERMAL SENSOR

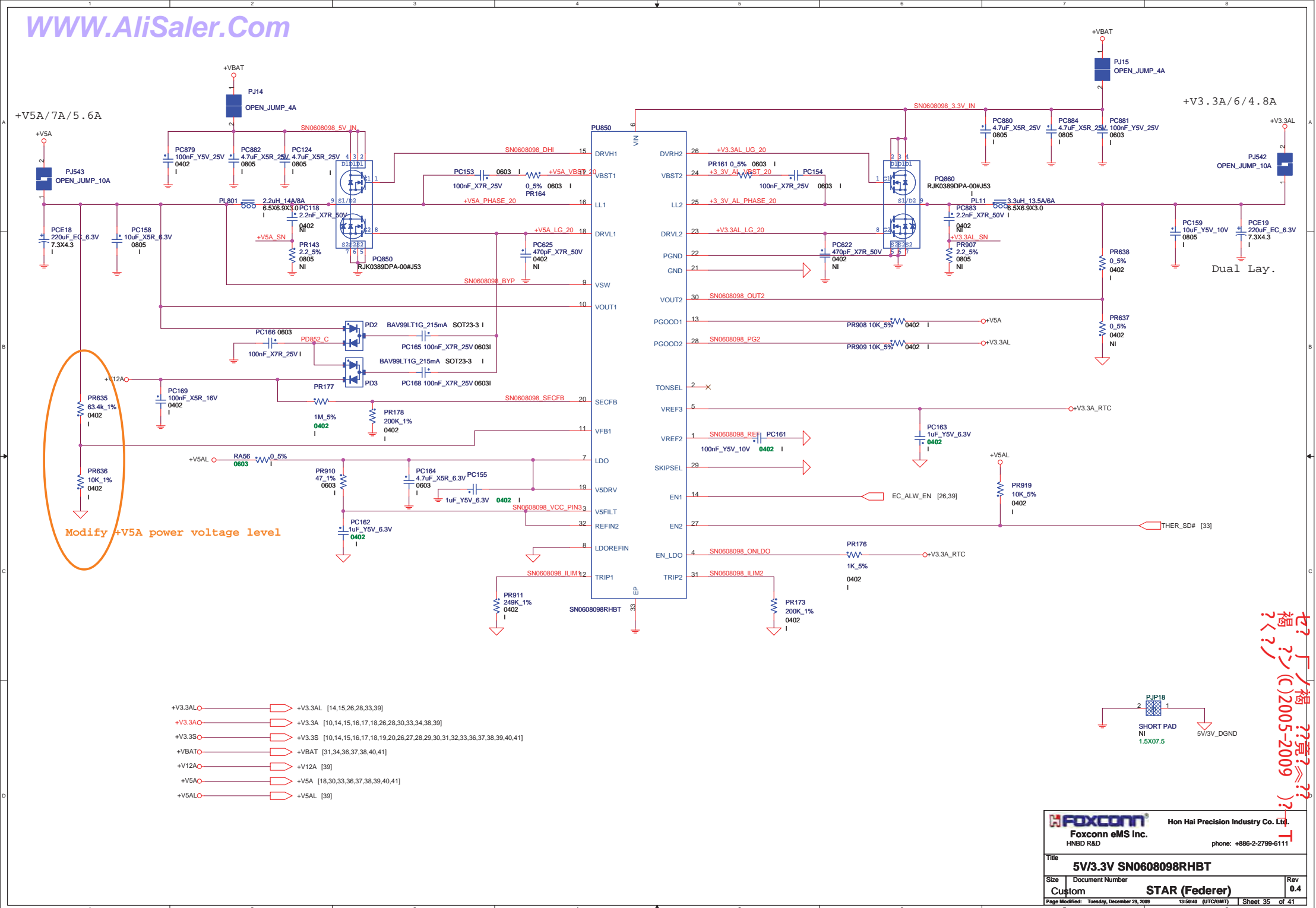


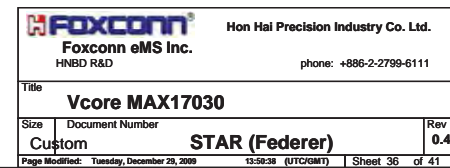
BATTERY CONNECTOR



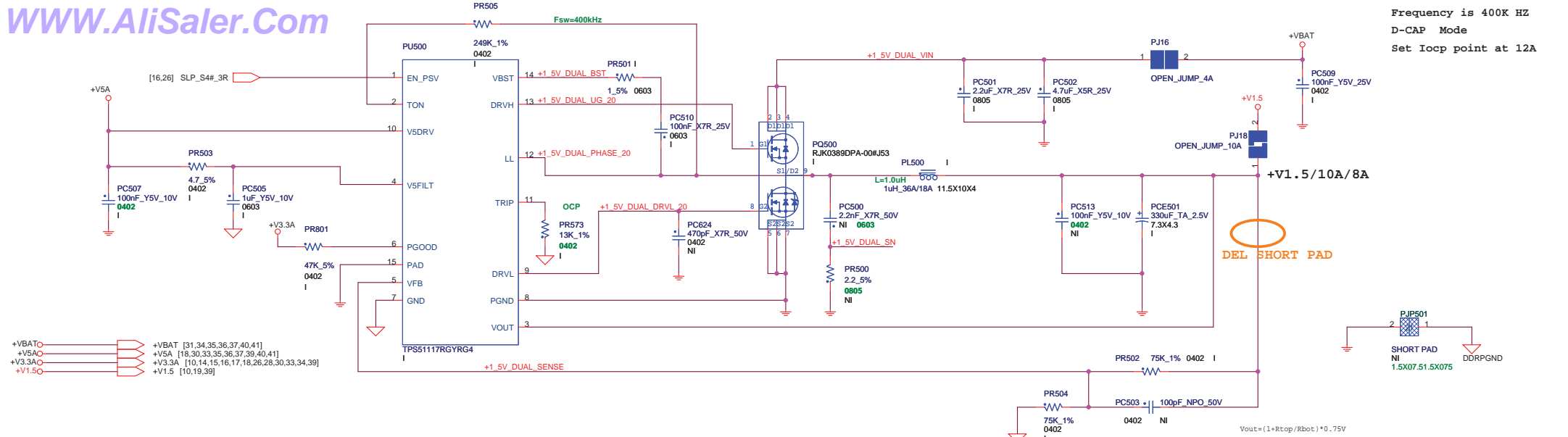
 Hon Hai Precision Industry Co. Ltd. Foxconn eMS Inc. HNBD R&D		phone: +886-2-2709-6111	
Title			
DCIN/Battery/OCPI/FAN			
Size	Document Number		
Custom	STAR (Federer)		
Procurement, Transfer, December 30, 1992		11/28/92 (11/28/92)	



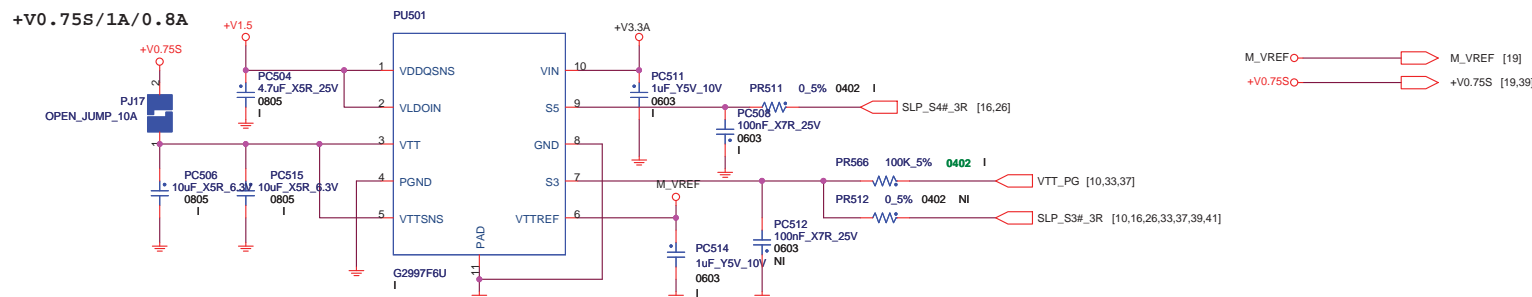
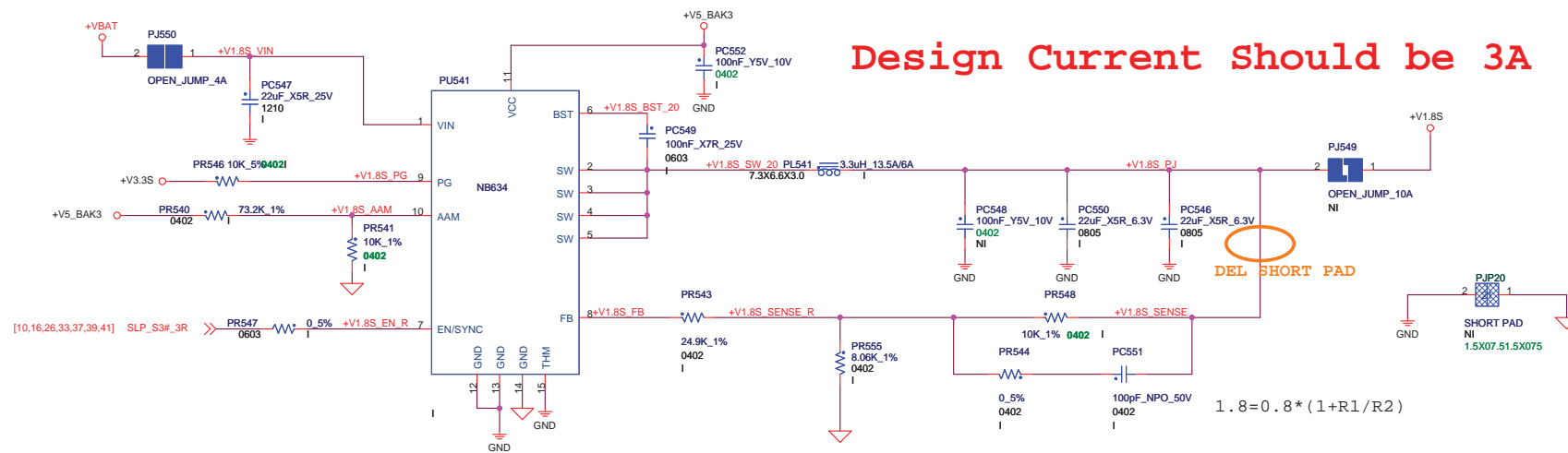


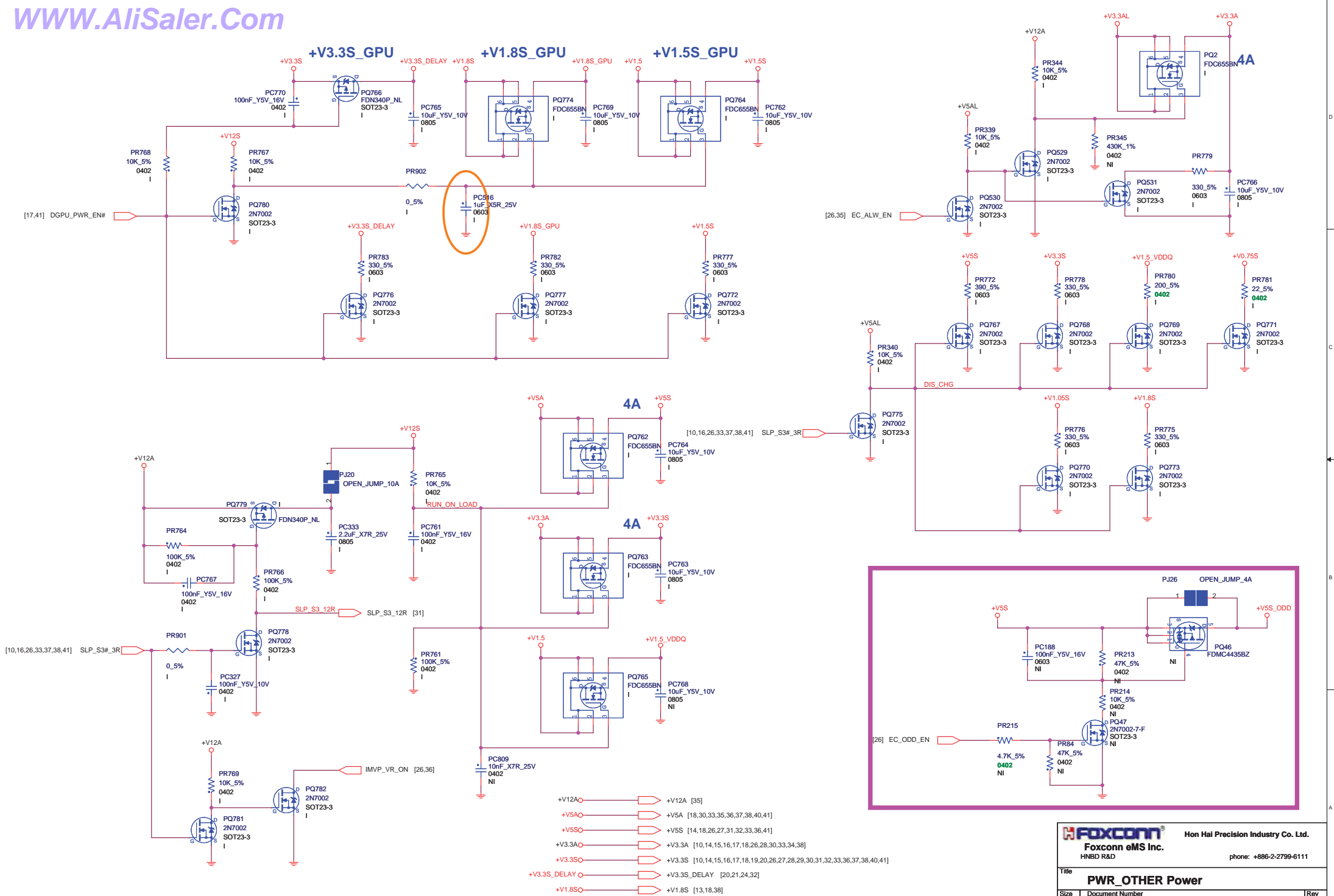


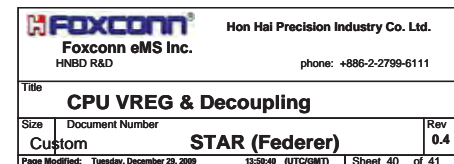


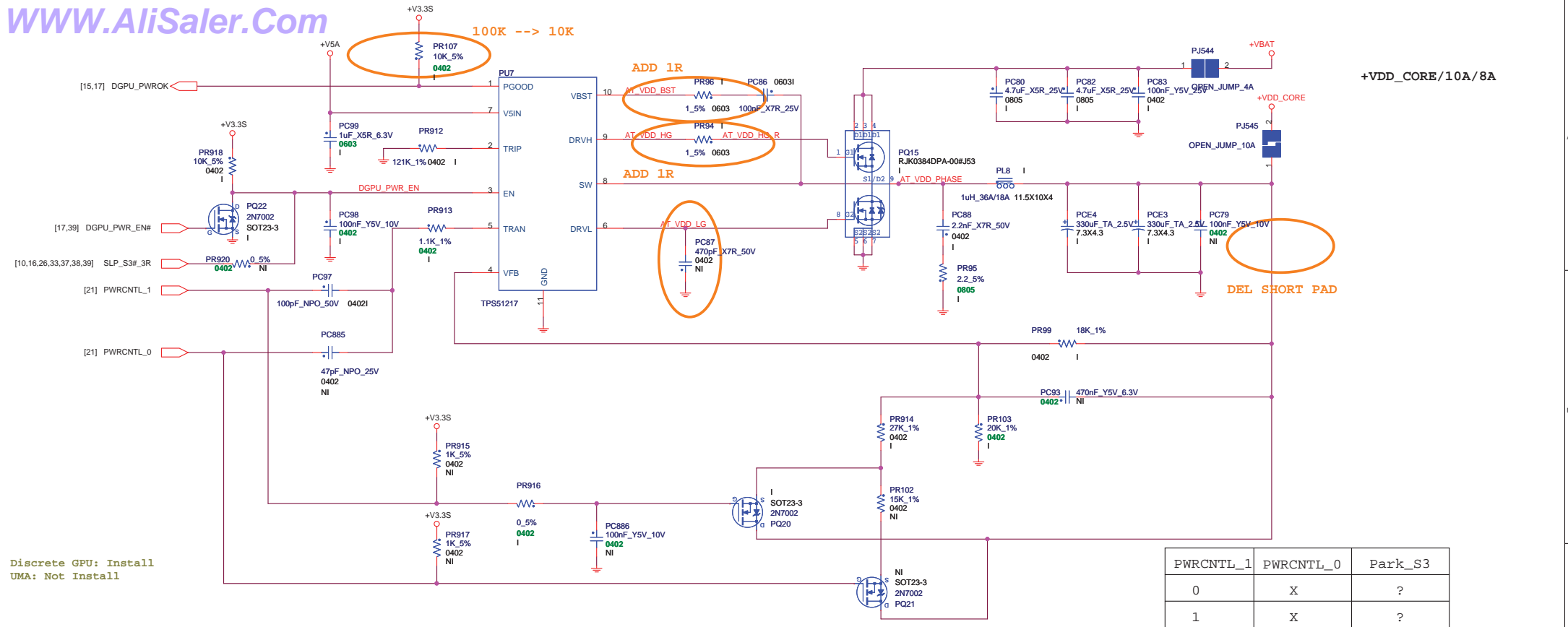


Design Current Should be 3A



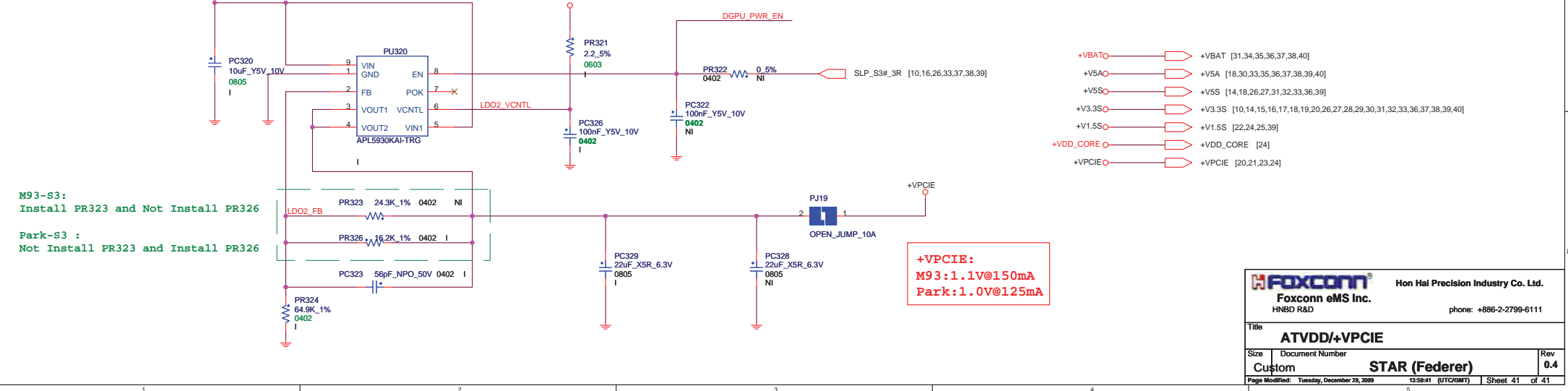






Discrete GPU: Install
UMA: Not Install

Discrete GPU: Install
UMA: Not Install



M93-S3:
Install PR323 and Not Install PR326

Park-S3 :
Not Install PR323 and Install PR326

+VPCIE:
M93: 1.1V@150mA
Park: 1.0V@125mA

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Foxconn eMS Inc.
HNBD R&D phone: +886-2-2799-6111

Title: **ATVDD/+VPCIE**

Size: Document Number
Custom **STAR (Federer)** Rev **0.4**

Page Modified: Tuesday, December 28, 2009 13:59:41 (UTC/GMT) Sheet 41 of 41